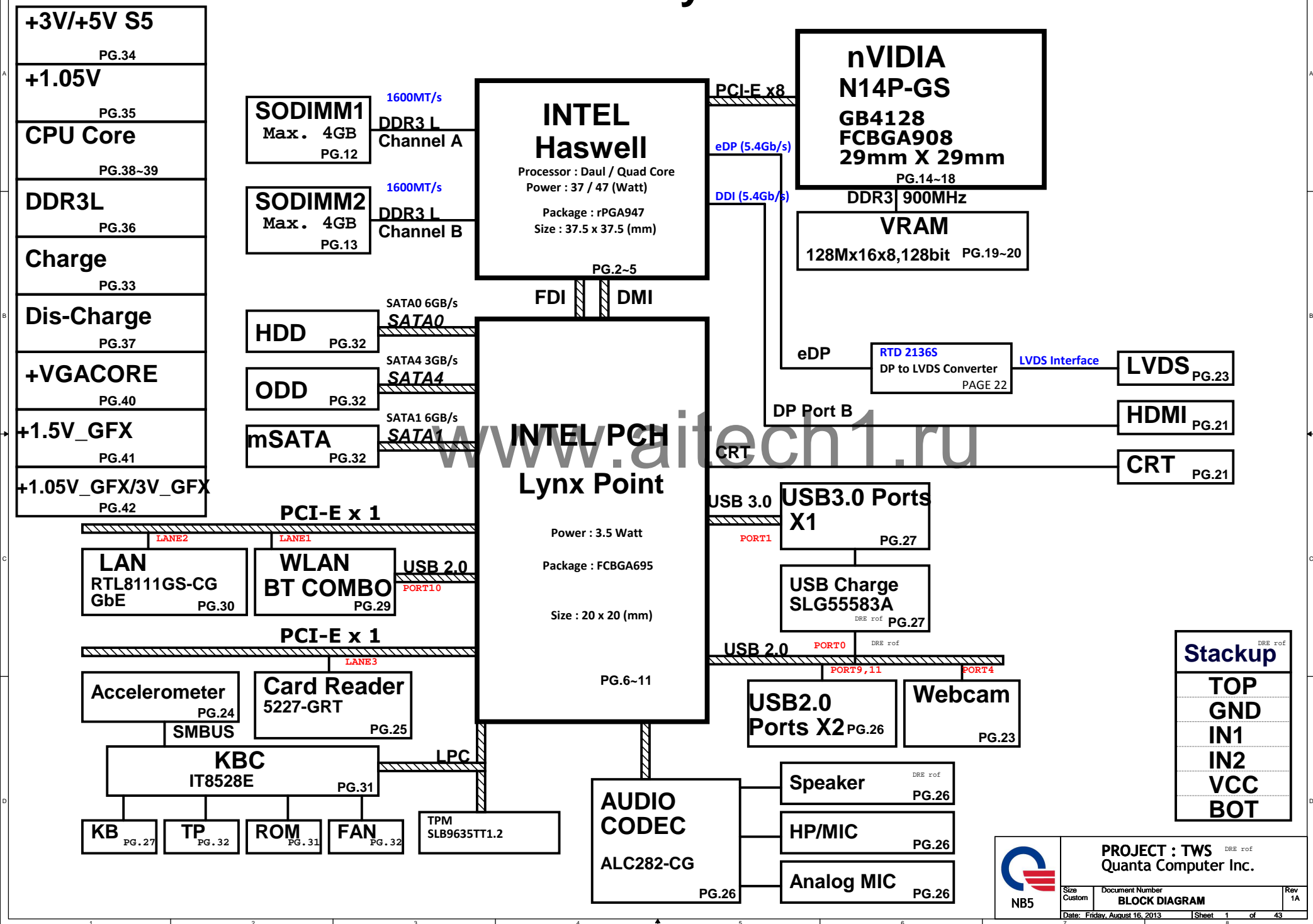
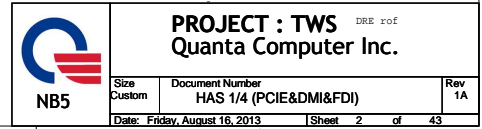


# TWS Shark Bay DIAGRAM

01

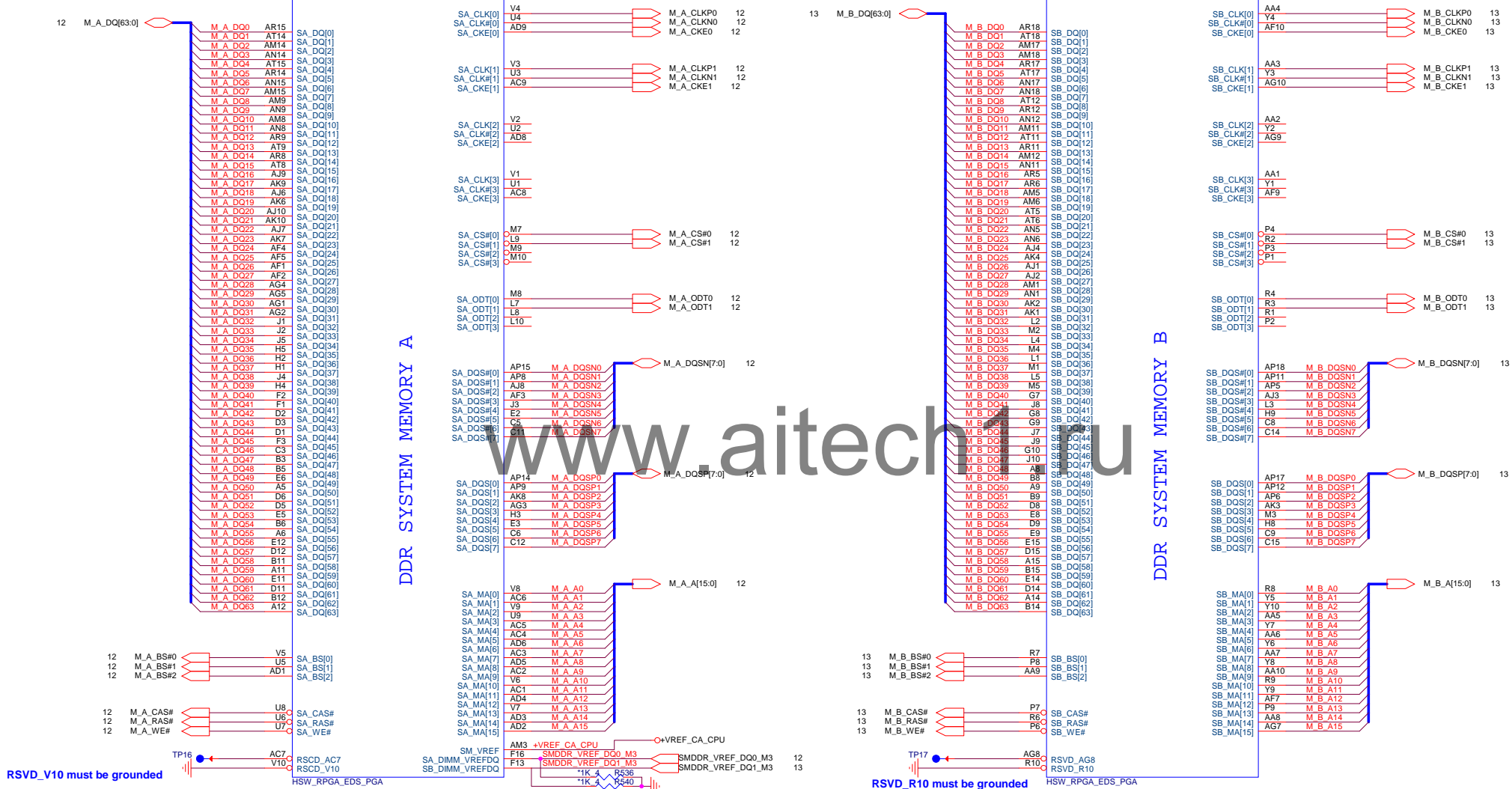




## Haswell Processor (DDR3)

U23C

U23D



CPU SM\_VREF

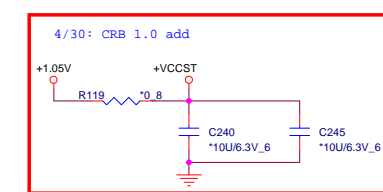
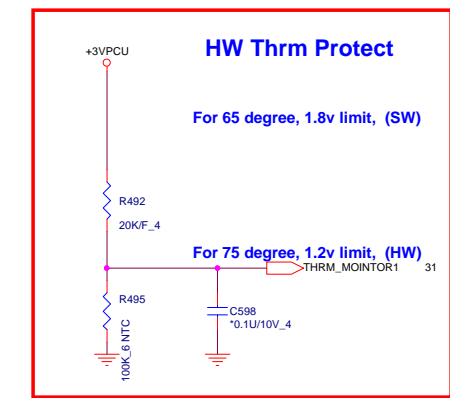
# Haswell Processor (POWER)

04

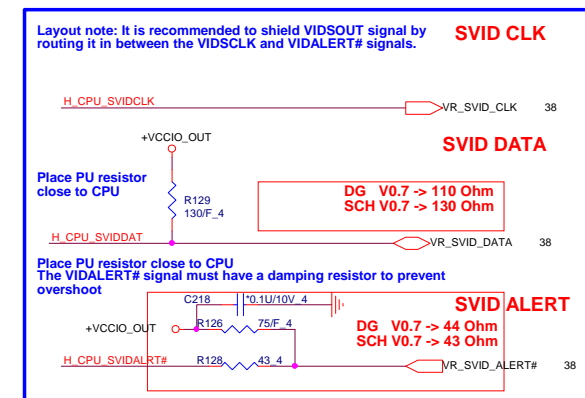
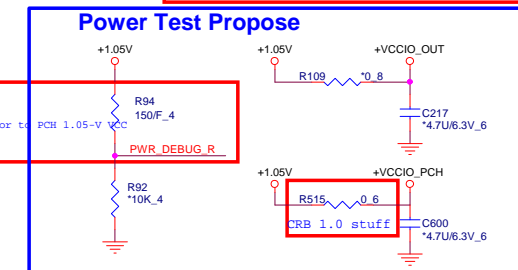


VDDQ Output Decoupling Recommendations		
330uFx2	7343	BOT socket side
22uFx11	0805	5 on TOP, 6 on BOT inside socket cavity
10uFx10	0805	5 on TOP, 5 on BOT inside socket cavity

+VCCIOA_OUT	2
+VCCIO_OUT	2,38
+VCCIO_PCH	10
+1.5V	6,7,8,10,26,29,32,36
+1.05V	2,9,10,27,35,42
+VCC_CORE	38,39
+VCCST	2
+1.35VSUS	2,12,13,36



4/30: DG 498550  
Haswell PWR\_DEBUG requires a 150-ohm pull-up resistor to Core when routed to XDP



**CPU VDDQ**

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**Quanta Computer Inc.**

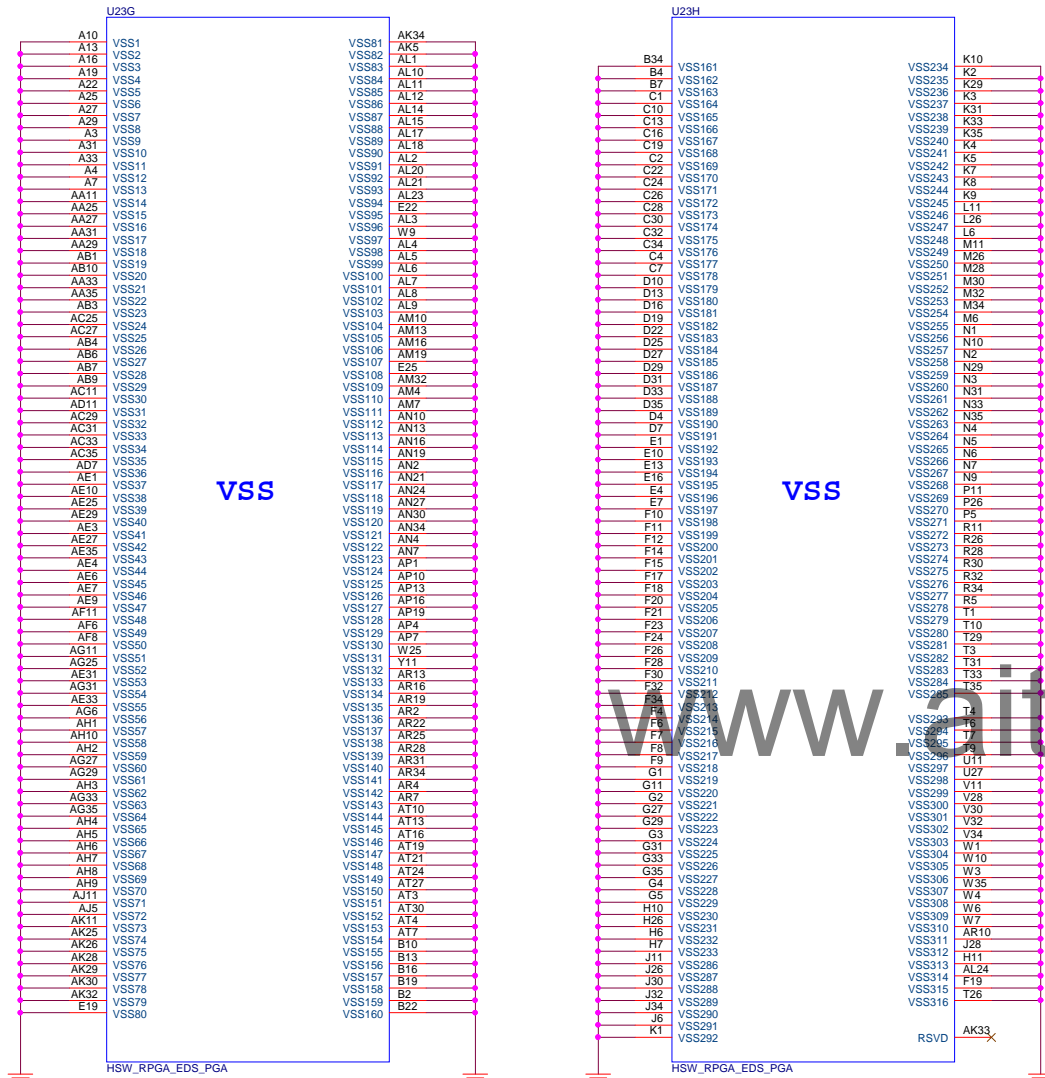
**NBS**

Size	Document Number	Rev
Custom	HAS 3/4 (POWER)	1A

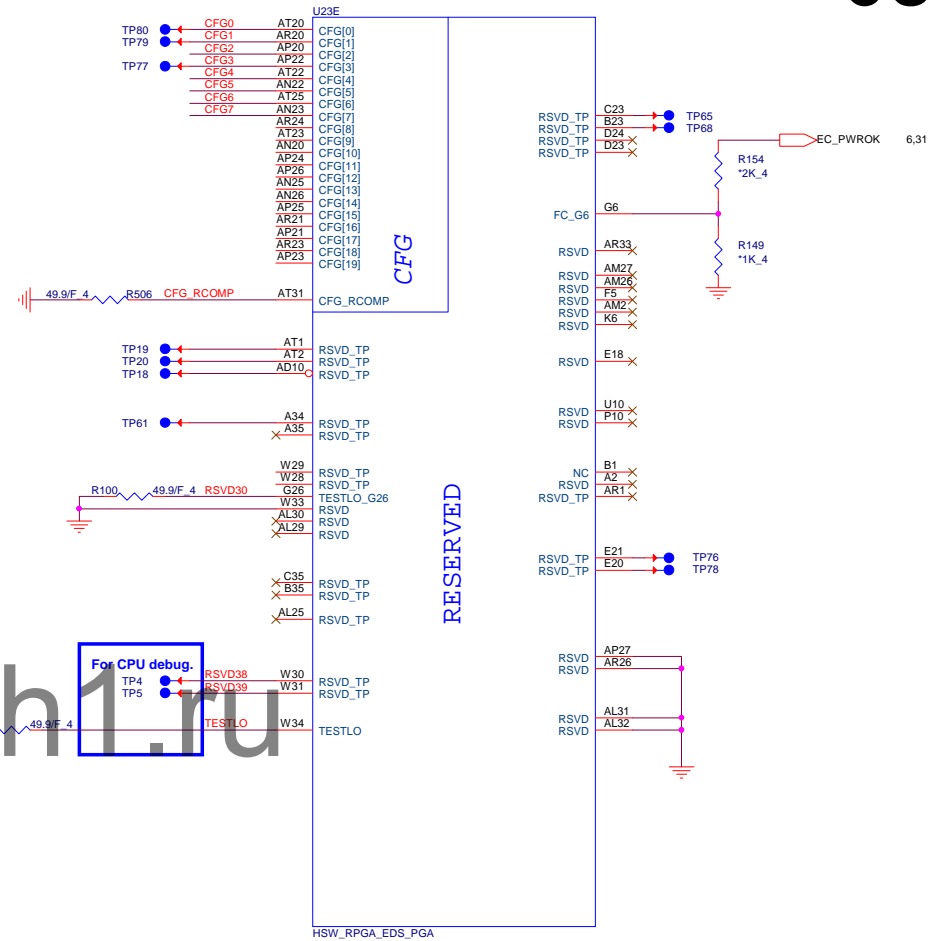
Date: Friday, August 16, 2013 | Sheet 4 of 43



## Haswell Processor (GND)



## Haswell Processor (RESERVED, CFG)



## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

## CFG[3] (PHYSICAL\_DEBUG\_ENABLED (DFX PRIVACY))

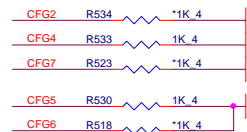
0 Enable; SET DFX ENABLED BIT IN DEBUG

1, Disable;

CFG3 R524 \*1K 4

## CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled  
 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled  
 01: Reserved - (Device 1 function 1 disabled; function 2 enabled)  
 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled



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Size Custom	Document Number HAS 4/4 (GND)	Rev 1A
Date: Friday, August 16, 2013		Sheet 5 of 43



### System PWR\_OK(CLG)



+	+3V_DEEP_SUS	7,8,9,10,29
+	+3V_RTC	7,10,27
+	+1.05V	2,4,9,10,27,35,42
+	+3VPCU	4,27,29,31,32,33,34
+	+3VSS	2,7,9,10,24,27,28,29,31,34,36,37,42
+	+3V	2,7,8,9,10,12,13,14,17,21,22,23,24,25,26,28,29,30,31,32,37,38,40
+	+5V	21,26,28,29,32,37,40

On Die DSW VR Enable
High = Enable (Default) Low = Disable



**PROJECT : TWS**  
**Quanta Computer Inc.**

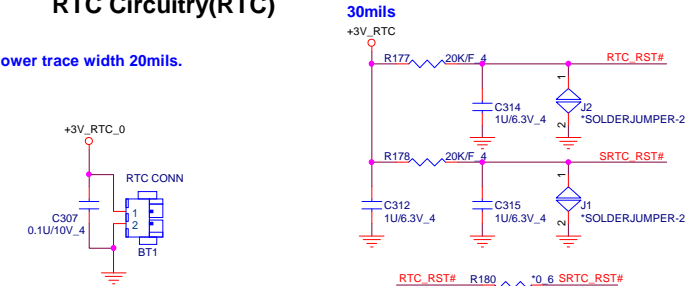
Size Custom	Document Number PCH 1/6 (DMI/FDI/VIDEO)
----------------	--

+	1.05V	2,4,9,10,27,35,42
+	3V_RTC	6,10,27
+	3VPCU	4,27,29,31,32,33,34
+	3V	2,6,8,9,10,12,13,14,17,21,22,23,24,25,26,28,29,30,31,32,37,38,40
+	3V_DEEP_SUS	6,8,9,10,29
+	5V	21,26,28,29,32,37,40

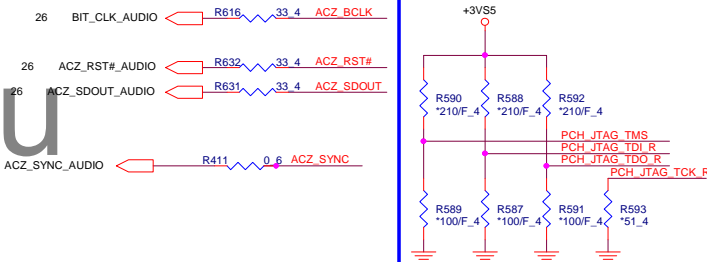
07

2  
2  
3 **ODD (SATA1 1.5Gb/s)**

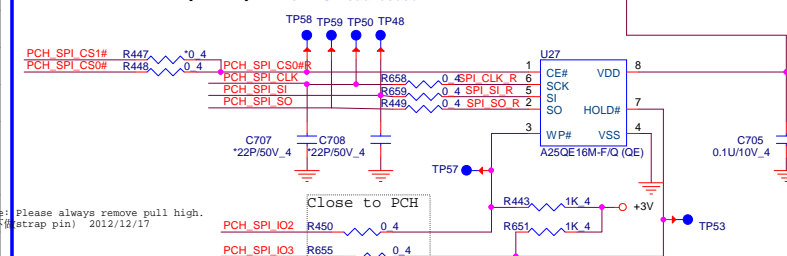
RTC Power trace width 20mils.



## PCH JTAG Debug(CLG)



If EC support embedded flash , SPI power must be used S5\_ON power rail for EC load code.



Vender	Size	P/N
AMIC	2MB	AKE38ZN0803 ( A25QE16M-F/Q (QE)
WIN	2MB	AKE38FP0N03 (W25Q16DVSSIQ)
Socket		DFHS08FS023

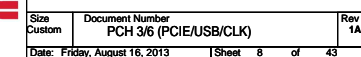


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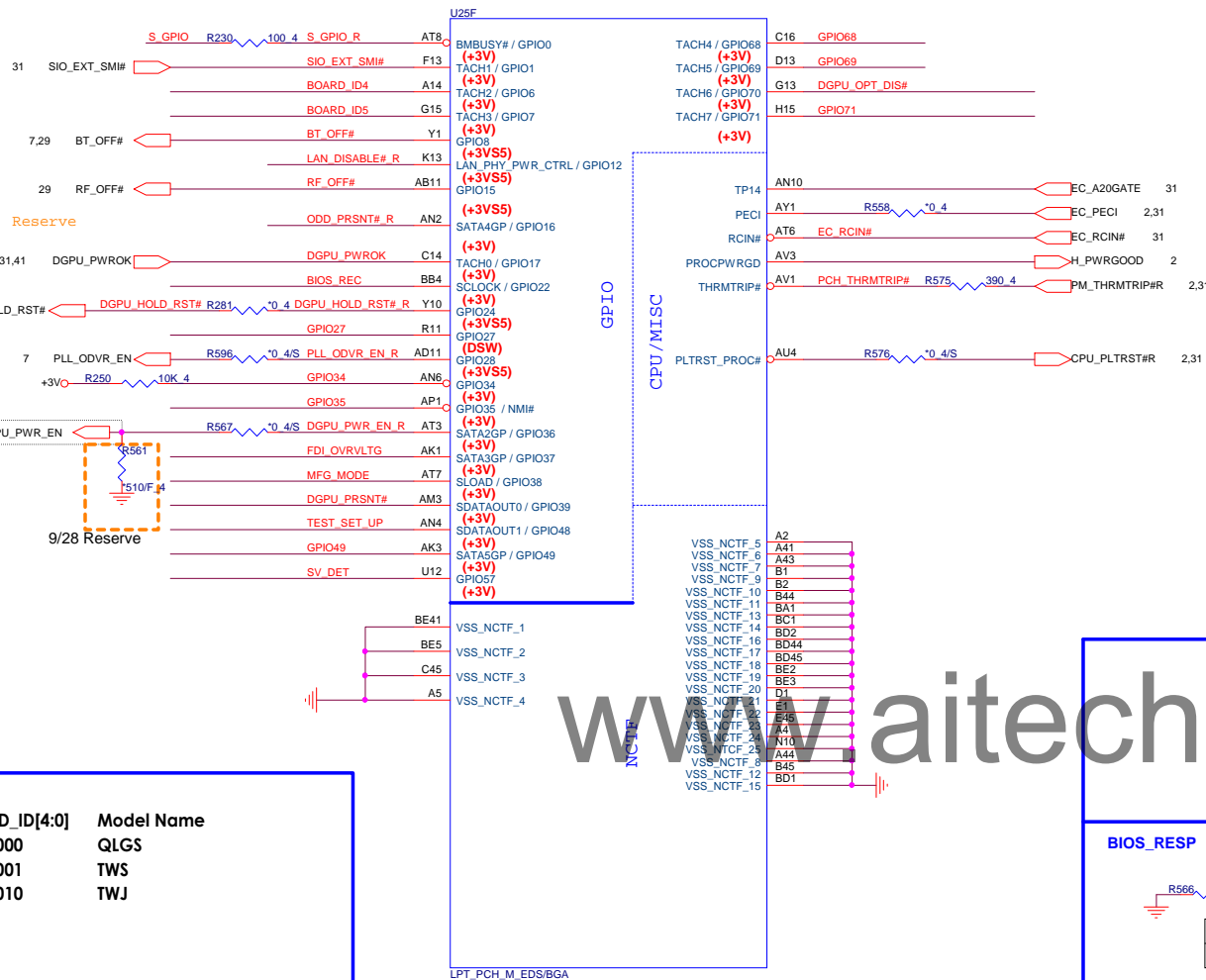
Size Custom	Document Number PCH 2/6 (SATA/HDA/SPI)	Rev. 1
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[illegible]

Pin Name	Strap description	Sampled	Configuration	Circuit									
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (Int PU)										
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	0 = Disable 1 = Enable										
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)										
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <thead> <tr> <th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr> </thead> <tbody> <tr> <td>1</td><td>1</td><td>SPI</td></tr> <tr> <td>0</td><td>0</td><td>LPC</td></tr> </tbody> </table>	GNT1#	GNT0#	Boot Location	1	1	SPI	0	0	LPC	<p>[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#</p>
GNT1#	GNT0#	Boot Location											
1	1	SPI											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK											
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V										
HDA_SDO	Flash Descriptor Security	PWROK	0 = Security Effect (Int PD) 1 = Can be Overridden										
GPIO8	RSVD	RSMRST#	Internal PU										
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Int PU)										
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable										
SUSCLK# / GPIO62	On-die PLL Voltage Regulator	PWROK	0 = Disable 1 = Enable (Int PU)										



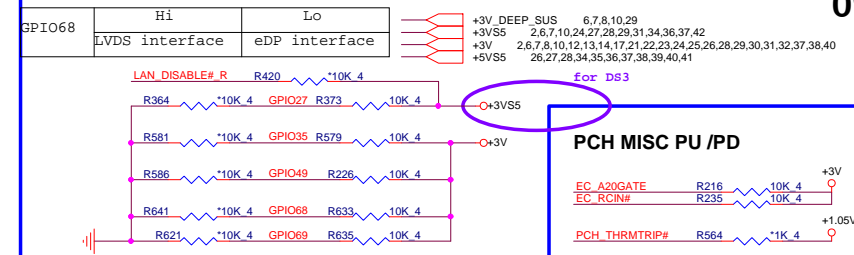
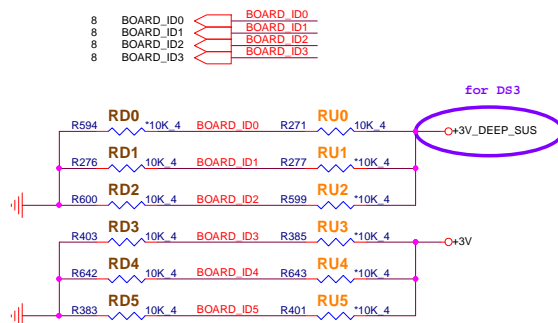
# Lynx Point (GPIO,VSS\_NCTF,RSVD)



BOARD_ID[4:0]	Model Name
00000	QLGS
00001	TWS
00010	TWJ

## HSW BOARD ID SETTING

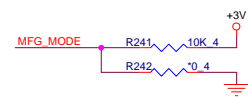
BOARD_ID0	GPIO44	MODEL_BIT0
BOARD_ID1	GPIO45	MODEL_BIT1
BOARD_ID2	GPIO46	MODEL_BIT2
BOARD_ID3	GPIO4	MODEL_BIT3
BOARD_ID4	GPIO6	MODEL_BIT4
BOARD_ID5	GPIO7	No Dolby=0, Dolby=1
GPIO71	GPIO71	Reserve
GPIO35	GPIO35	Reserve
GPIO49	GPIO49	Reserve
GPIO68	GPIO68	Reserve
GPIO69	GPIO69	Reserve
DGPU_PRSTNT	GPIO39	Optimus=1, UMA=0
DGPU_OPT_DIS#	GPIO70	Optimus=0, Dis only=1



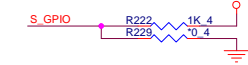
## PCH MISC PU/PD



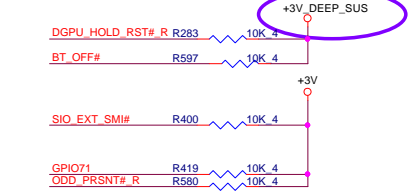
## MFG-TEST



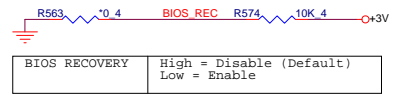
## Swap GPIO



## GPIO Pull-up/Pull-down(CLG)

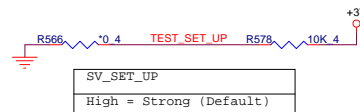


## DGPU\_PWROK UMA=0



BIOS RECOVERY	High = Disable (Default)	Low = Enable
---------------	--------------------------	--------------

## BIOS\_RESP



SV_SET_UP
High = Strong (Default)

## SV Detect

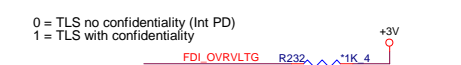


SV Detect	0 = SV Detect	1 = Default
-----------	---------------	-------------

## DGPU\_OPT\_DIS# GPIO70 Optimus=0, Dis only=1

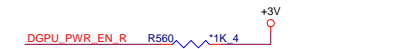


## SATA3GP/GPIO37 TLS Confidentiality

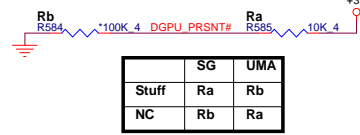


0 = TLS no confidentiality (Int PD)	1 = TLS with confidentiality
-------------------------------------	------------------------------

## GPIO36 Internal PD



## GFX Present GPIO39 Optimus=1, UMA=0



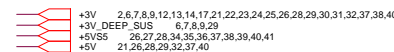
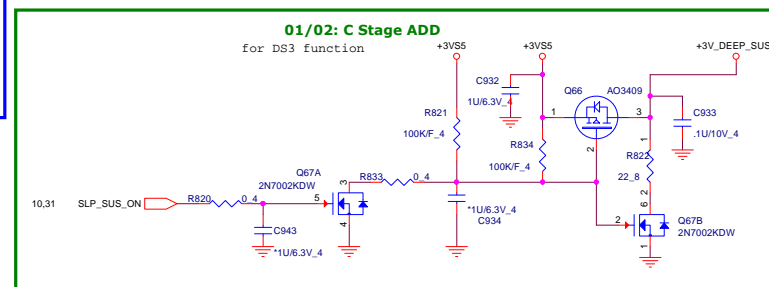
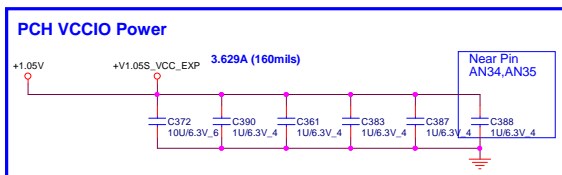
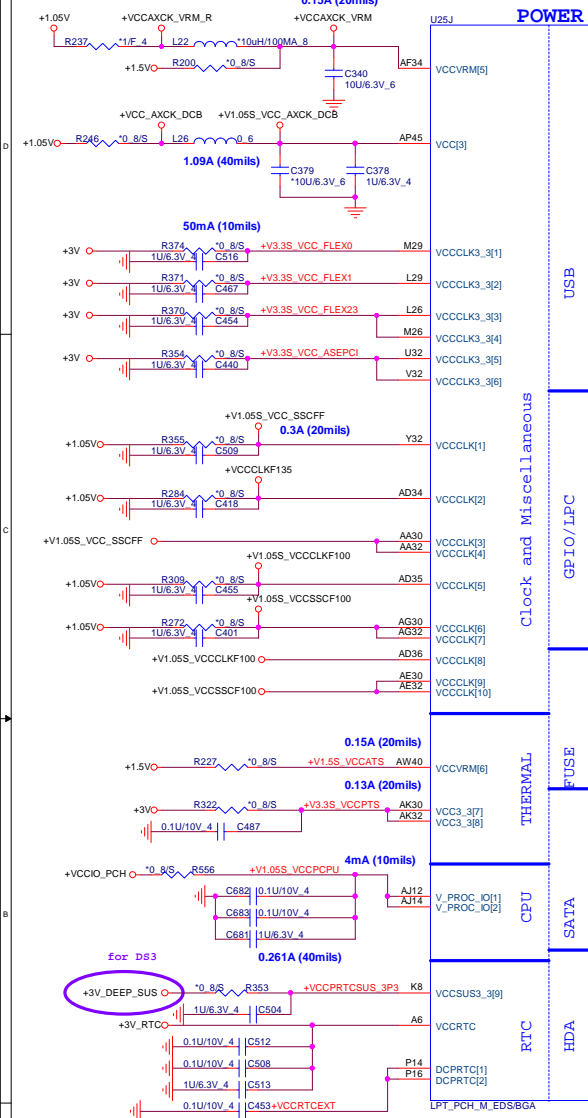
SG	UMA
Stuff	Ra
NC	Rb

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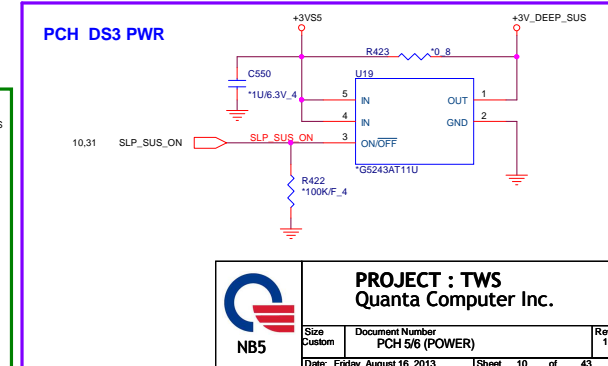
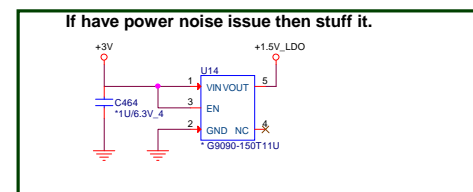
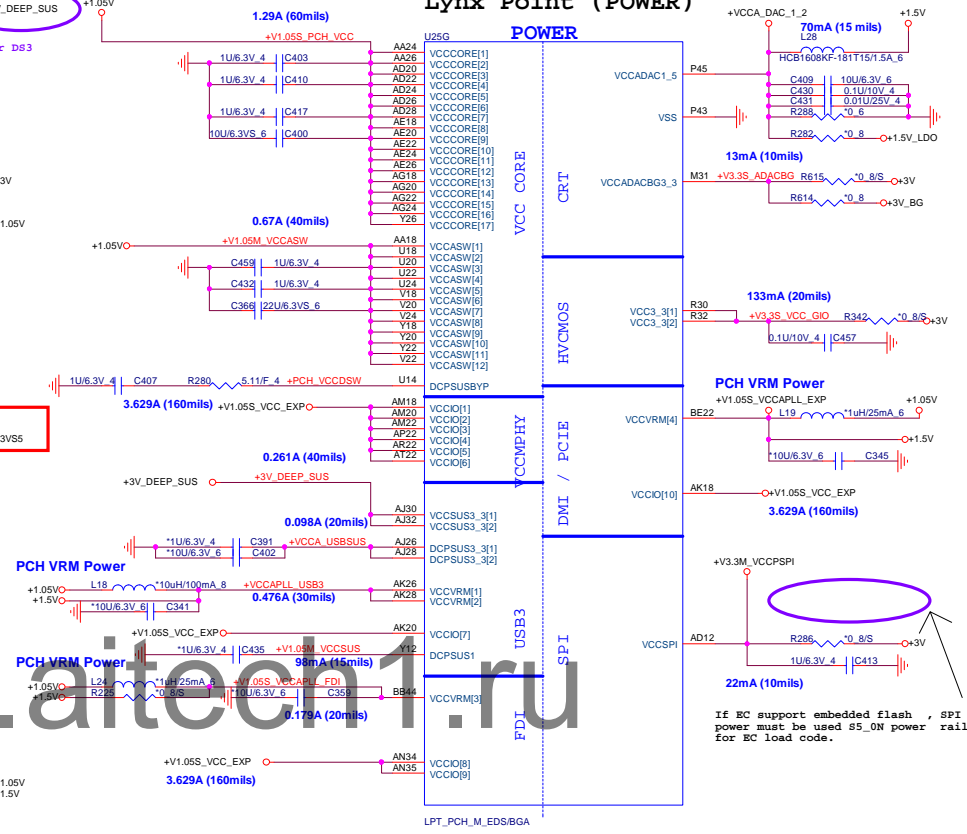
Size Custom	Document Number PCH 4/6 (GPIO/MISC)	Rev 1A
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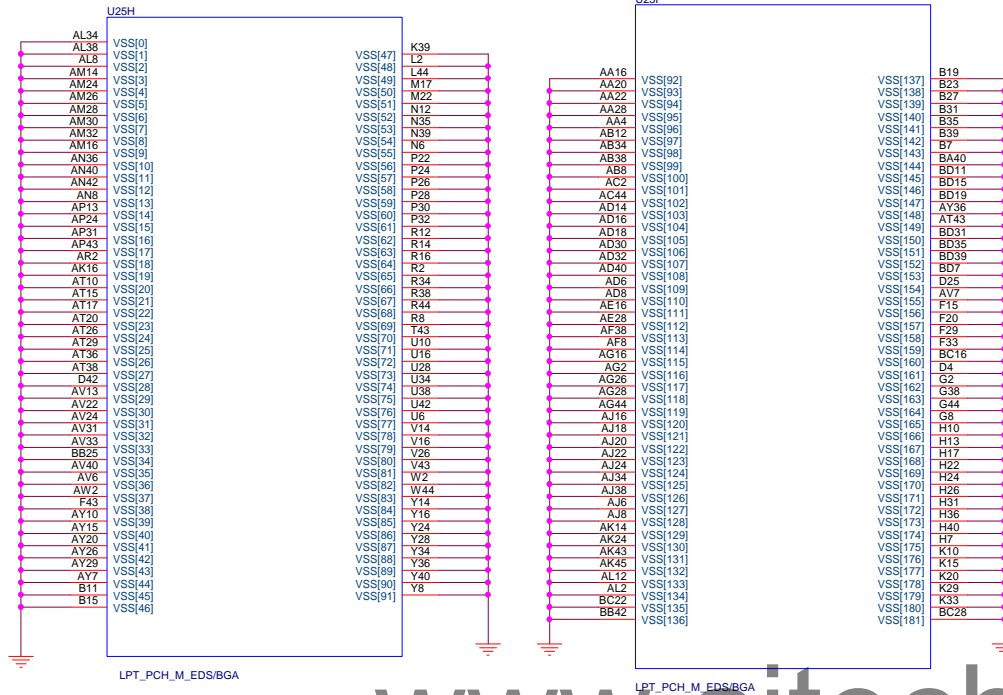
Lynx Point (POWER)



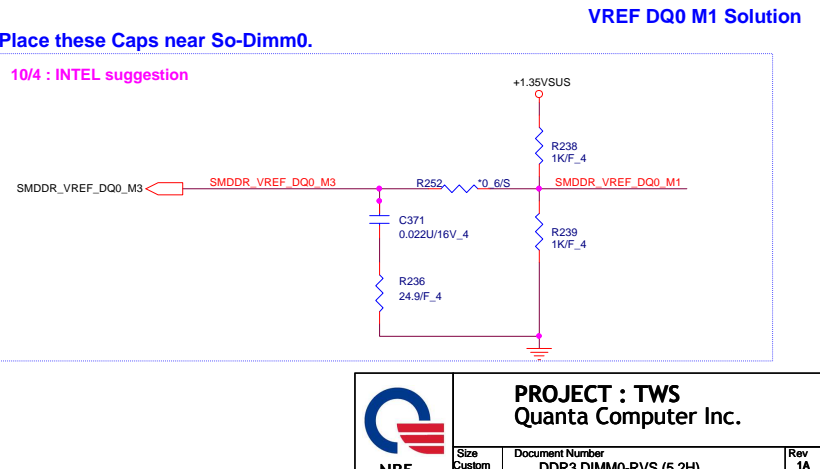
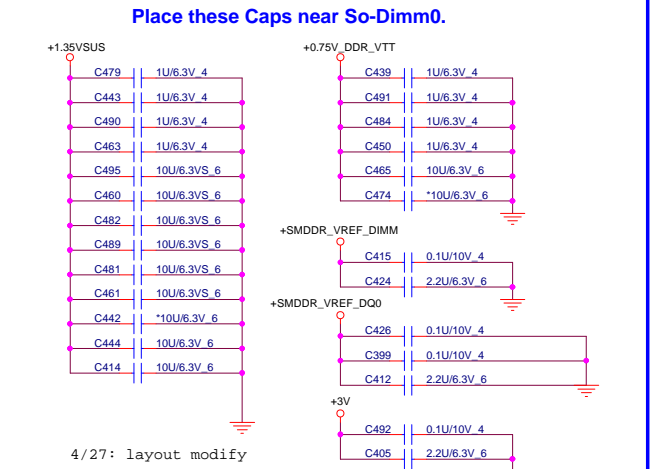
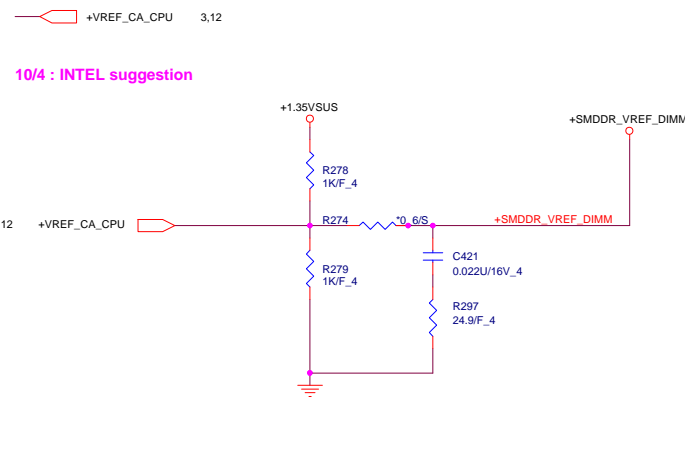
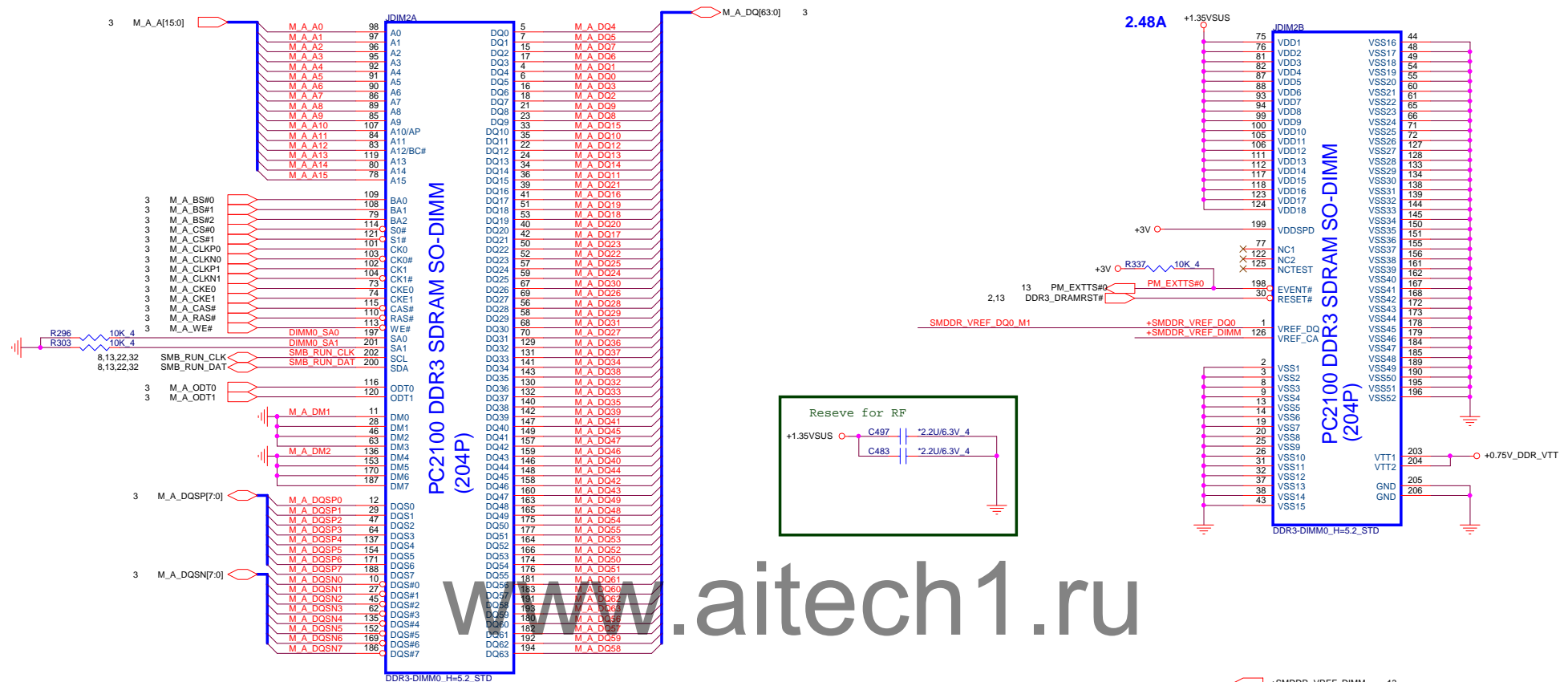
## Lynx Point (POWER)



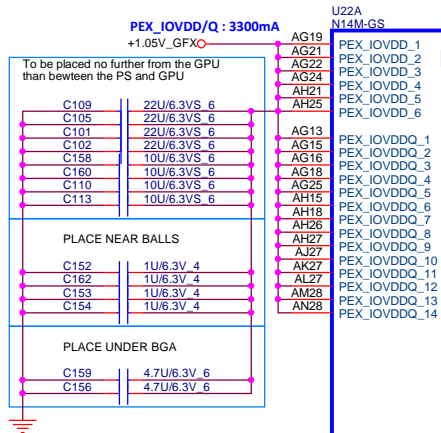
Lynx Point (GND)



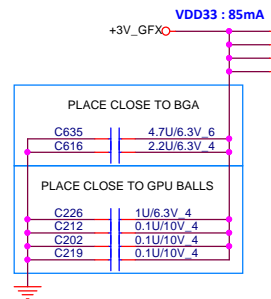
www.aitech1.ru



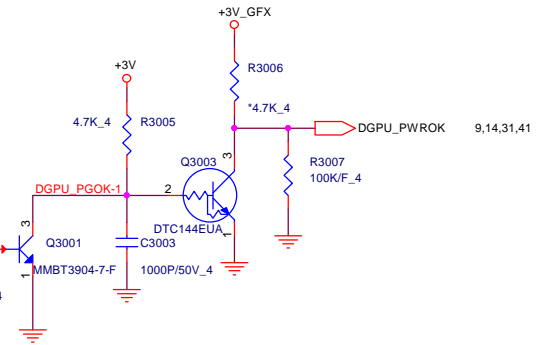
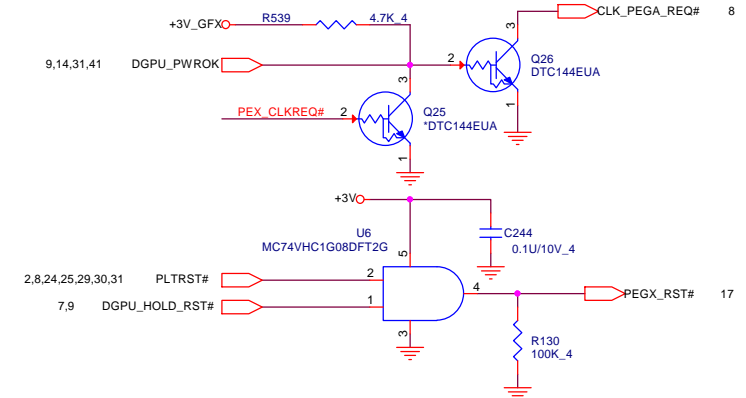
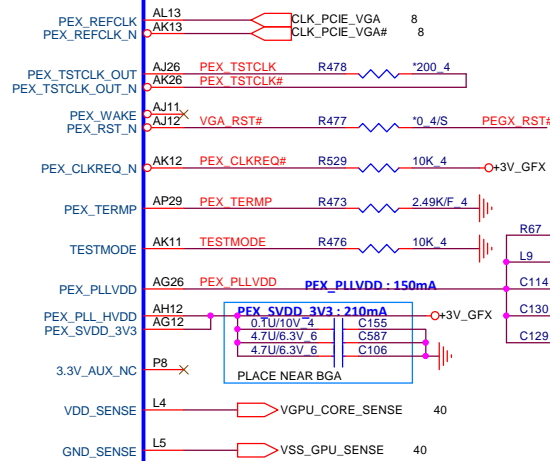
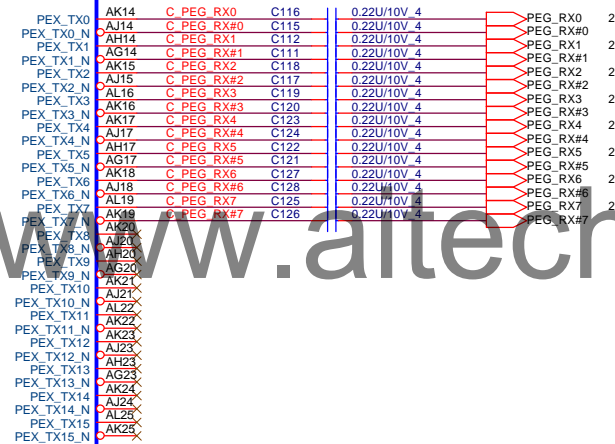
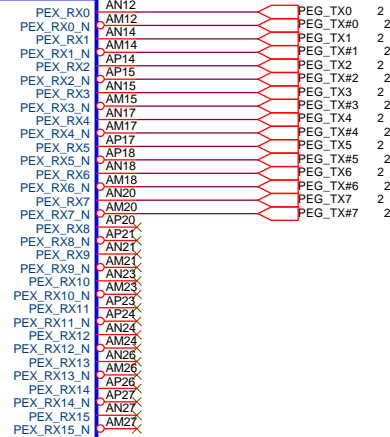




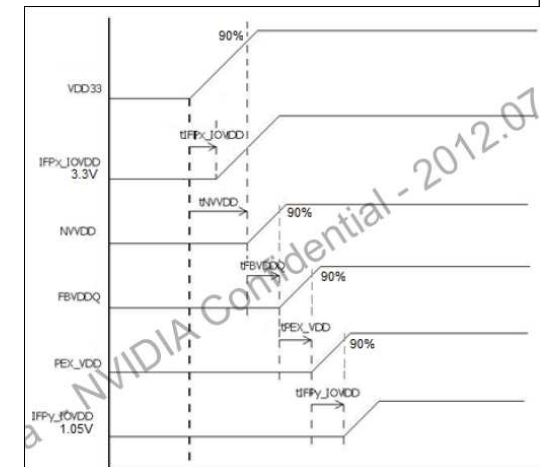
AC8 NC\_1  
AJ28 NC\_2  
AJ4 NC\_3  
AJ5 NC\_4  
AL11 NC\_5  
C15 NC\_6  
D19 NC\_7  
D20 NC\_8  
D23 NC\_9  
H31 NC\_10  
T8 NC\_11  
V32 NC\_12  
NC\_13



## PEG Interface



For DGPU\_PWROK sequence to early issue(B Stage)



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**Quanta Computer Inc.**

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A3	N14M-GS - 1/5 (PCIe)	1A
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17,18,42 +3V\_GFX  
15,18,19,20,41 +1.5V\_GFX  
15,16,42 +1.05V\_GFX  
2,6,7,8,9,10,12,13,17,21,22,23,24,25,26,28,29,30,31,32,37,38,40 +3V



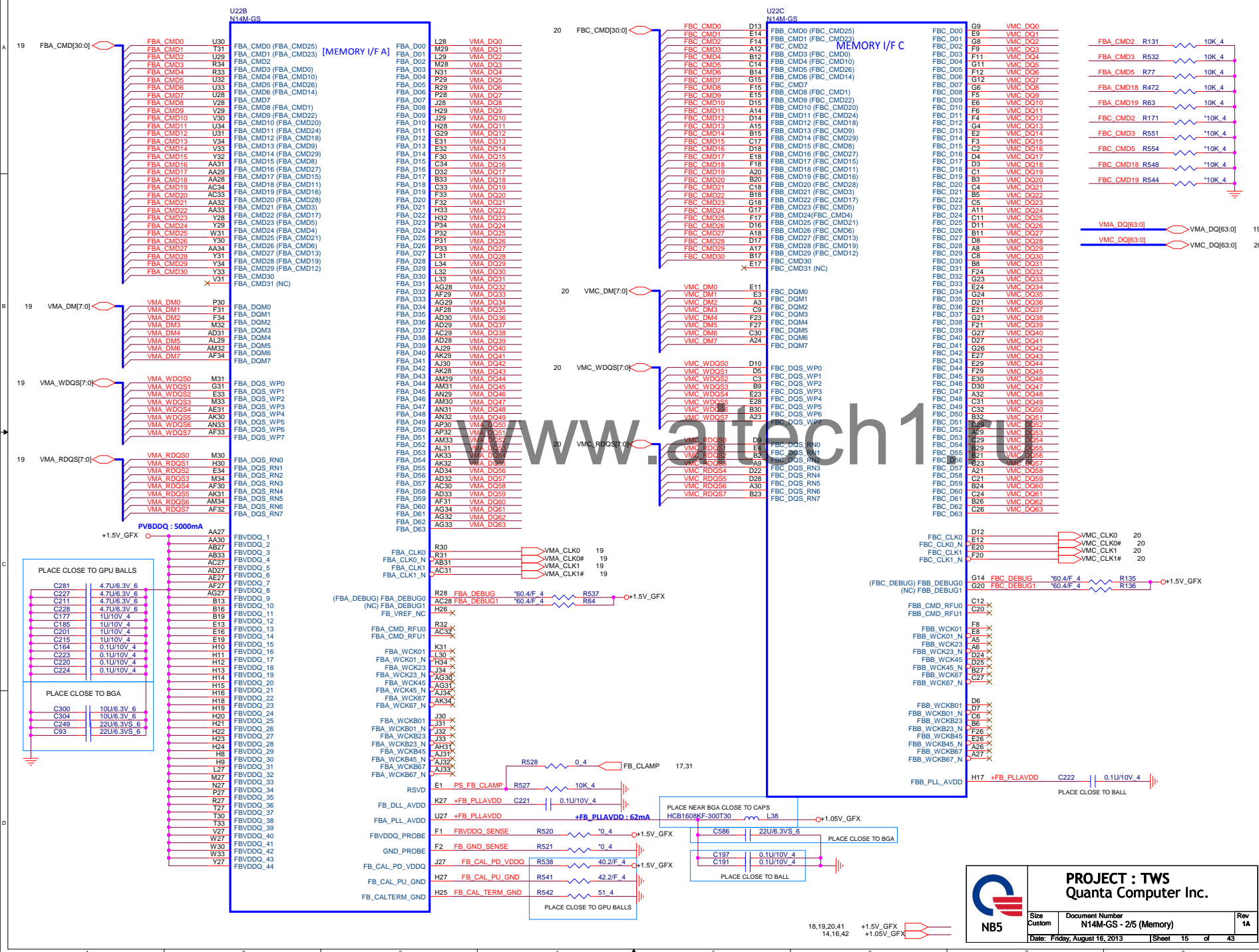


Table 3. N14M-GS/LP and N14P-GV2 DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
128Mx16 DDR3	Samsung	0x7	1.5 V/ 1.5 V	K4W2G1646E-BC1A	1000	1204	Production Candidate
				K4W2G1646E-BC11	900	1204	Production Candidate
	Micron	0x5	1.5 V/ 1.5 V	MT41J128M16JT-093G:K	1000	1234	Production Candidate
				MT41J128M16JT-107G:K	900	1150	Production Candidate
	Hynix	0x6	1.5V/ 1.5V	H5TQ2G63DFR-110C	1000	N/A	Production Candidate
				H5TQ2G63DFR-111C	900	N/A	Production Candidate
256Mx16 DDR3	Samsung	0x3	1.5 V/ 1.5 V	K4W4G1646B-HC11	900	N/A	Production Candidate
	Micron	0x1	1.5 V/ 1.5 V	MT41K256M16HA-107G:E	900	N/A	Production Candidate

Table 4. N14M-GS/LP and N14P-GV2 DDR3L Recommended Memories 128Mx16 Configuration.

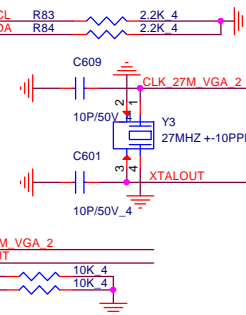
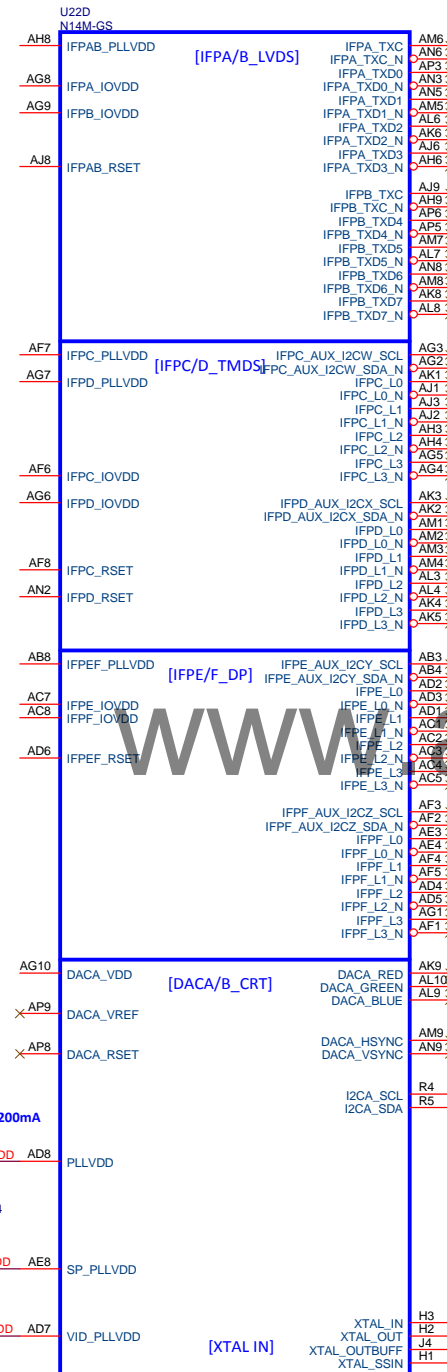
Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
128Mx16 DDR3L	Samsung	0xA	1.35 V/ 1.35 V	K4W2G1646E-BY11	900	1204	Production Candidate
	Micron	0x8	1.35 V/ 1.35 V	MT41K128M16JT-107G:K	900	N/A	Production Candidate

Table 5. N14P-GS/LP/GE/GT DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
128Mx16 DDR3	Samsung	0x7	1.5 V/ 1.5 V	K4W2G1646E-BC1A	1000	1204	Production Candidate
				K4W2G1646E-BC11	900	1204	Production Candidate
	Micron	0x5	1.5 V/ 1.5 V	MT41J128M16JT-093G:K	1000	1234	Production Candidate
				MT41J128M16JT-107G:K	900	1150	Production Candidate
	Hynix	0x6	1.5V/ 1.5V	H5TQ2G63DFR-110C	1000	N/A	Production Candidate
				H5TQ2G63DFR-111C	900	N/A	Production Candidate
256Mx16 DDR3	Samsung	0x3	1.5 V/ 1.5 V	K4W4G1646B-HC11	900	N/A	Production Candidate
	Micron	0x1	1.5 V/ 1.5 V	MT41K256M16HA-107G:E	900	N/A	Production Candidate

Table 6. N14P-GS/LP/GE/GT DDR3L Recommended Memories 128Mx16 Configuration.

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Date Code Minimum	Status
128Mx16 DDR3L	Samsung	0xA	1.35 V/ 1.35 V	K4W2G1646E-BY11	900	1204	Production Candidate
	Micron	0x8	1.35 V/ 1.35 V	MT41K128M16JT-107G:K	900	N/A	Production Candidate



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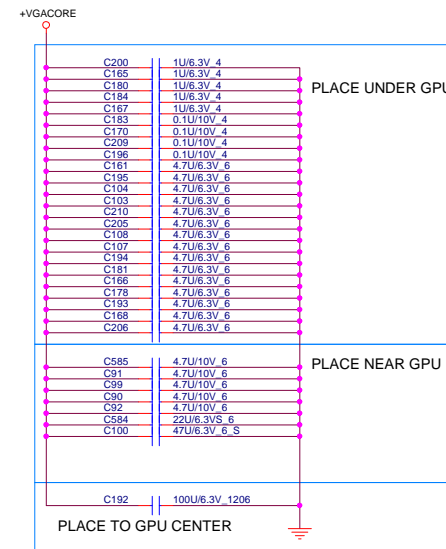
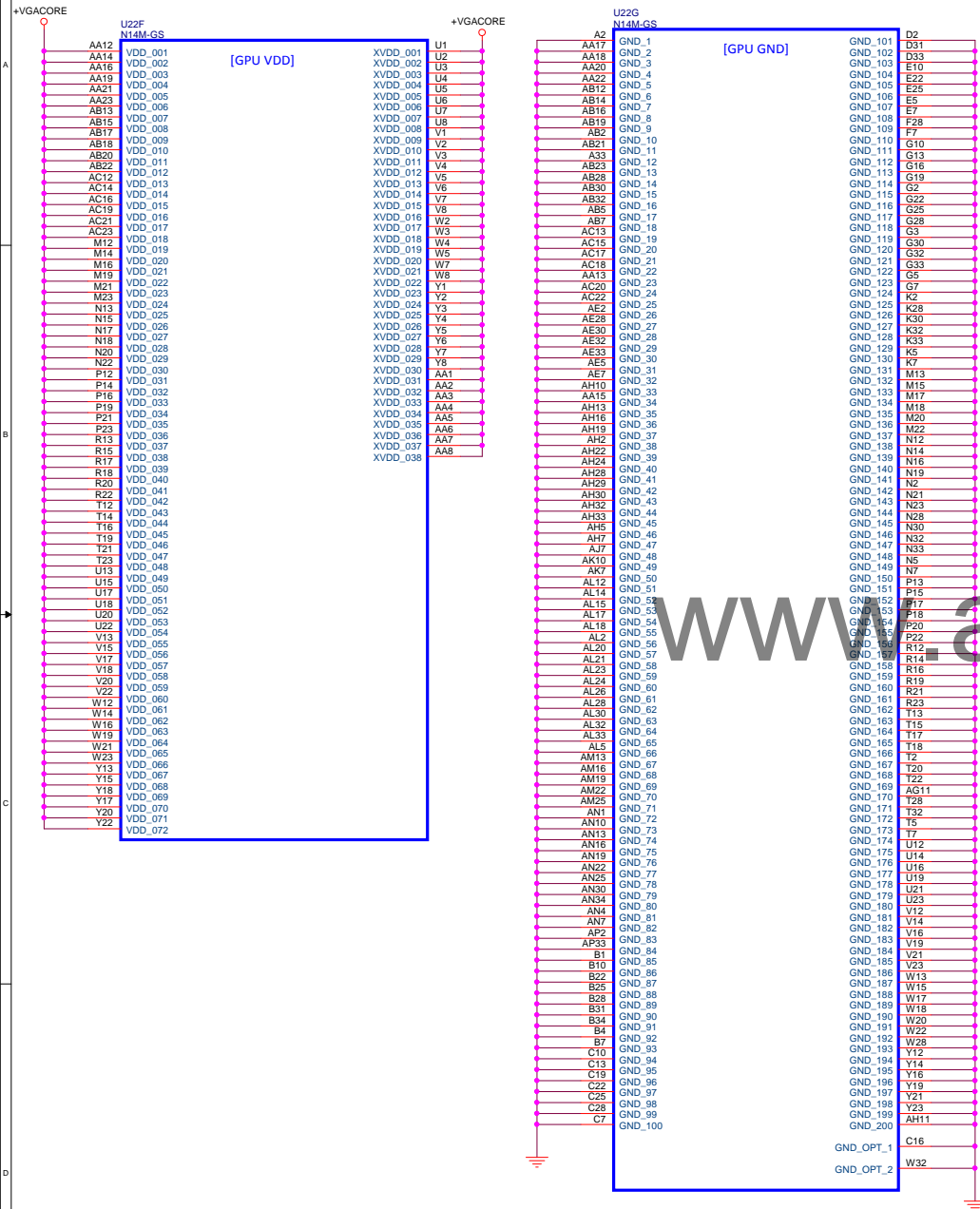
Size A3	Document Number N14M-GS - 3/5 (Display)	Rev 1A
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14,17,18,42  
14,15,42

+3V\_GFX  
+1.05V\_GFX



VDD/XVDD : 25.72A



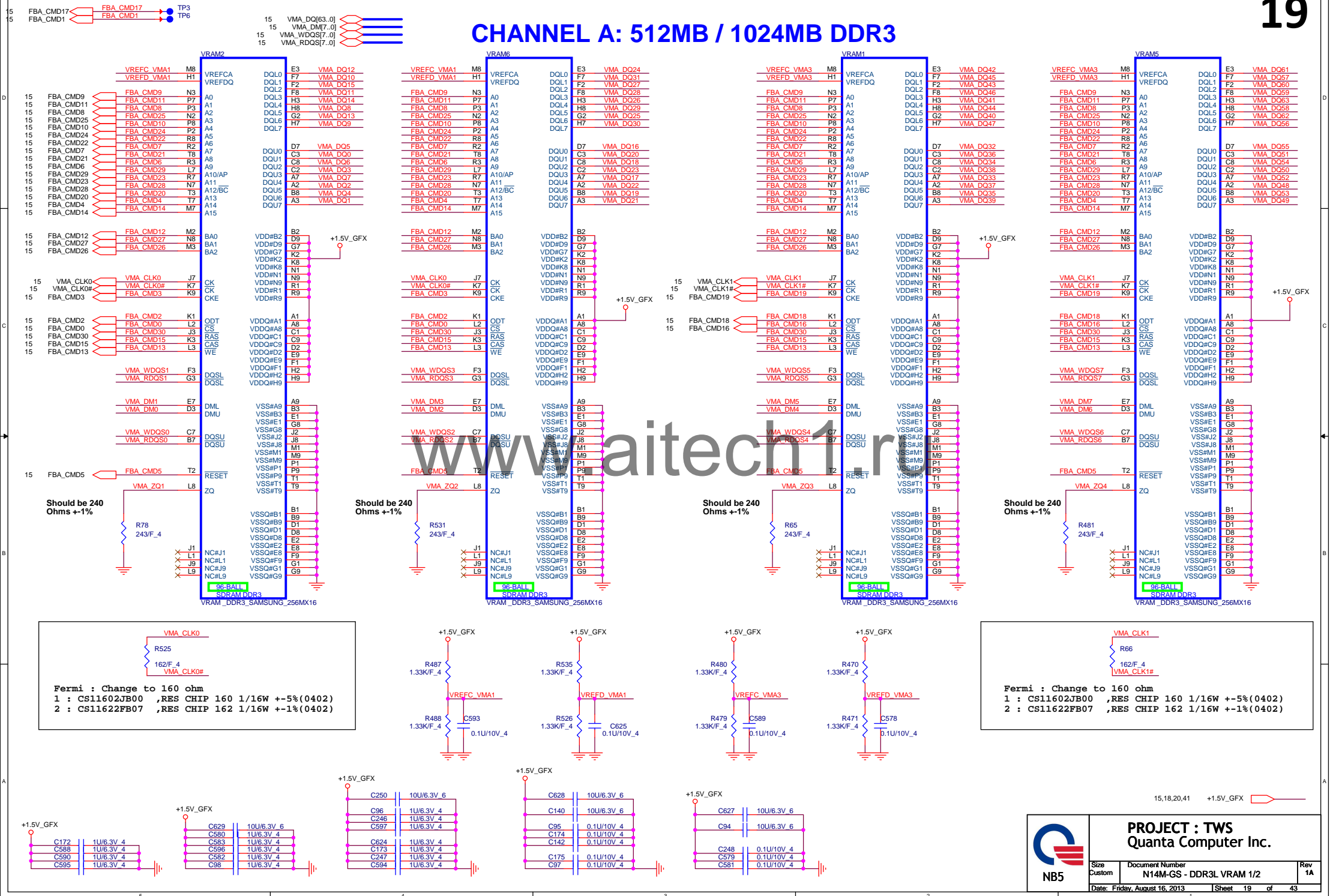
for meet Power down sequence for +3V\_GFX



120808 Del DGPU\_PWROK circuit  
because all +1.05V\_GFX/+1.5V\_GFX  
power solution have PG connector  
to PCH

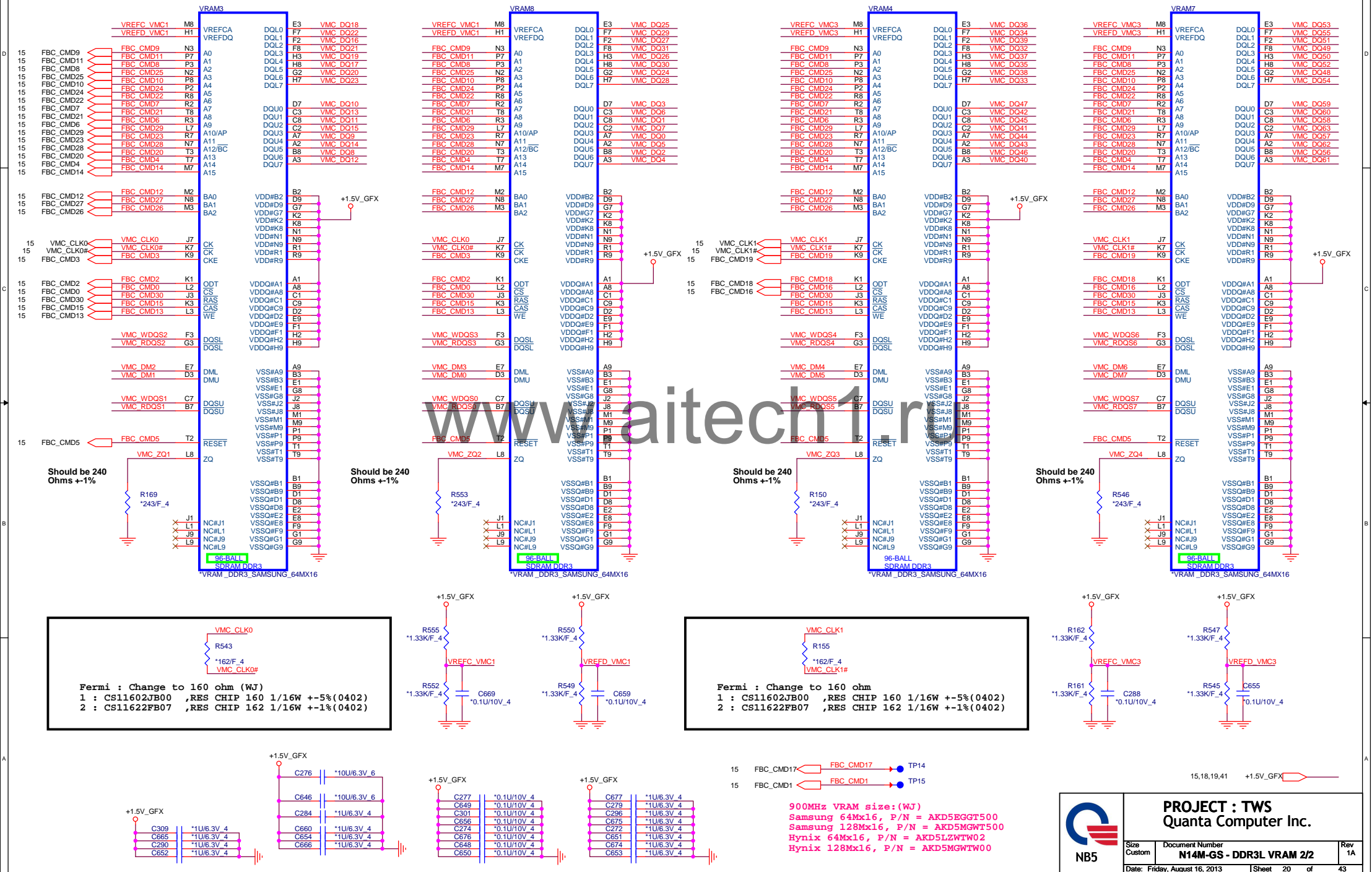


**CHANNEL A: 512MB / 1024MB DDR3**

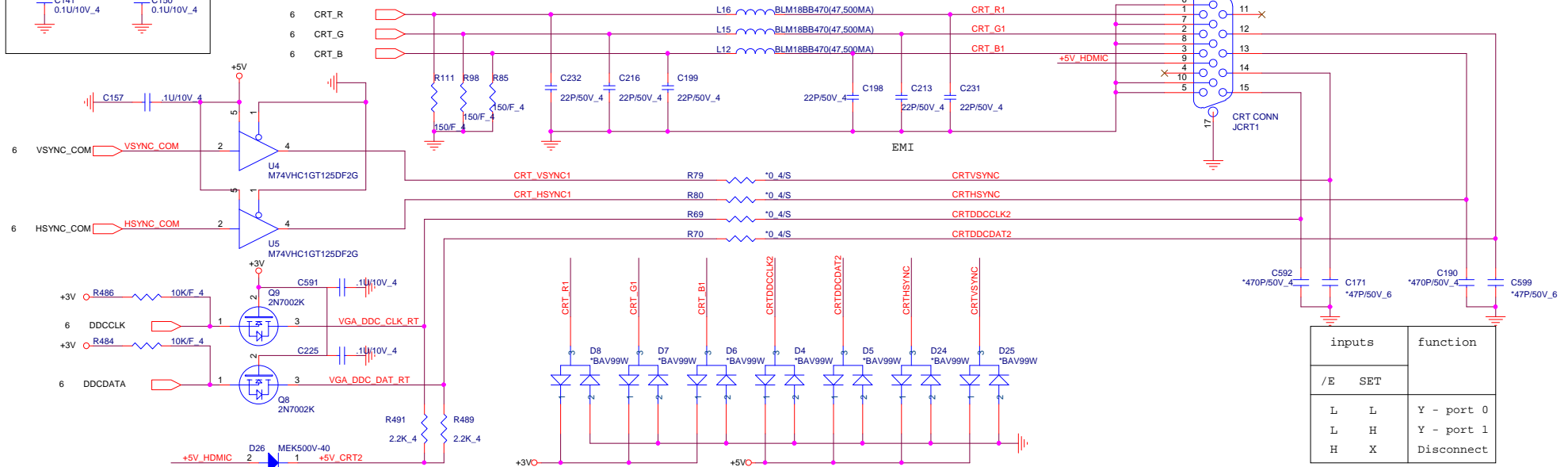




**CHANNEL B: 256MB/512MB DDR3**



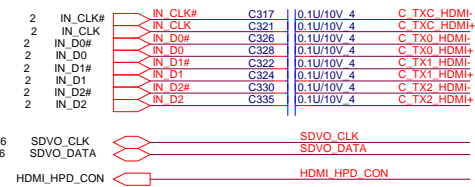
The diagram shows two decoupling capacitors, C141 and C150, connected to a +5V and +3V supply respectively. Both capacitors have a value of 0.1uF/10V\_4.



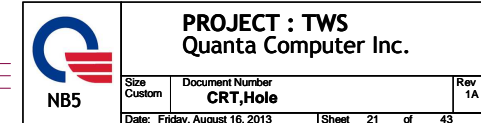
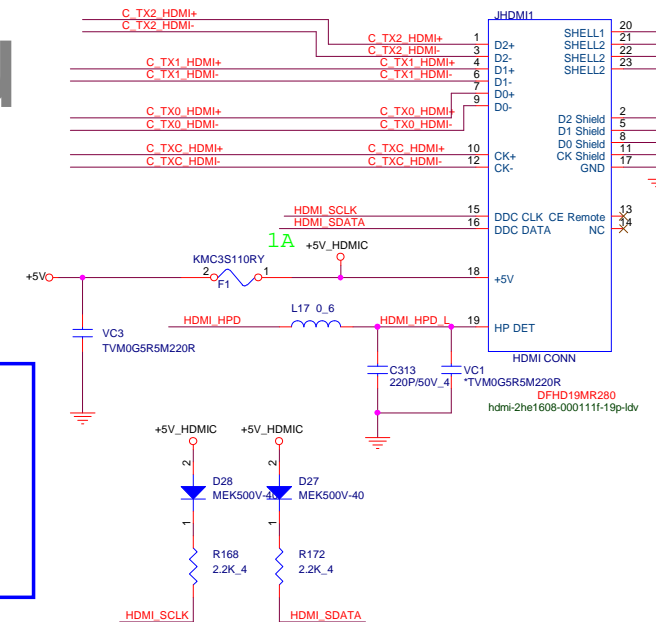
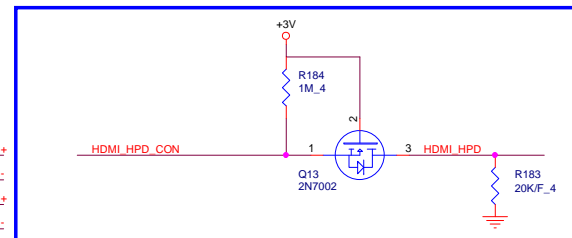
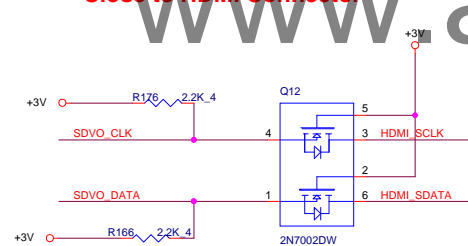
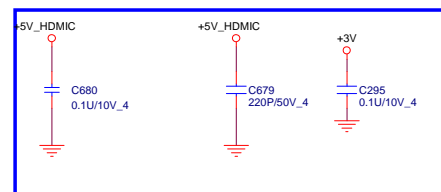
inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

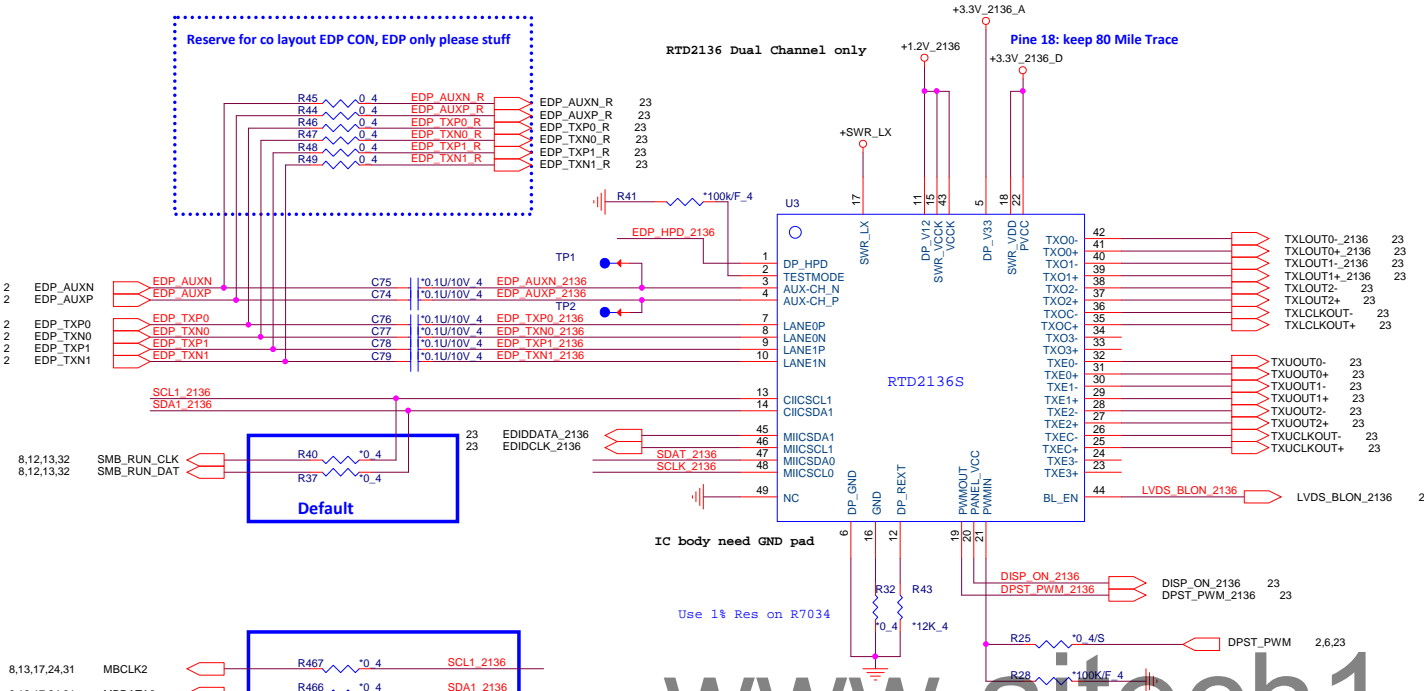
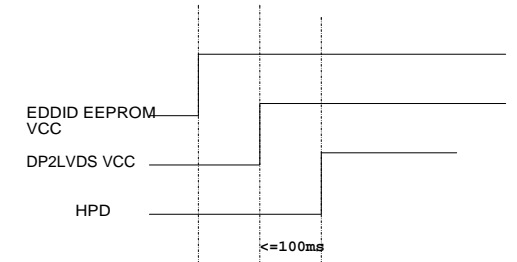
close to HDMI conn

**Close to HDMI Connector**



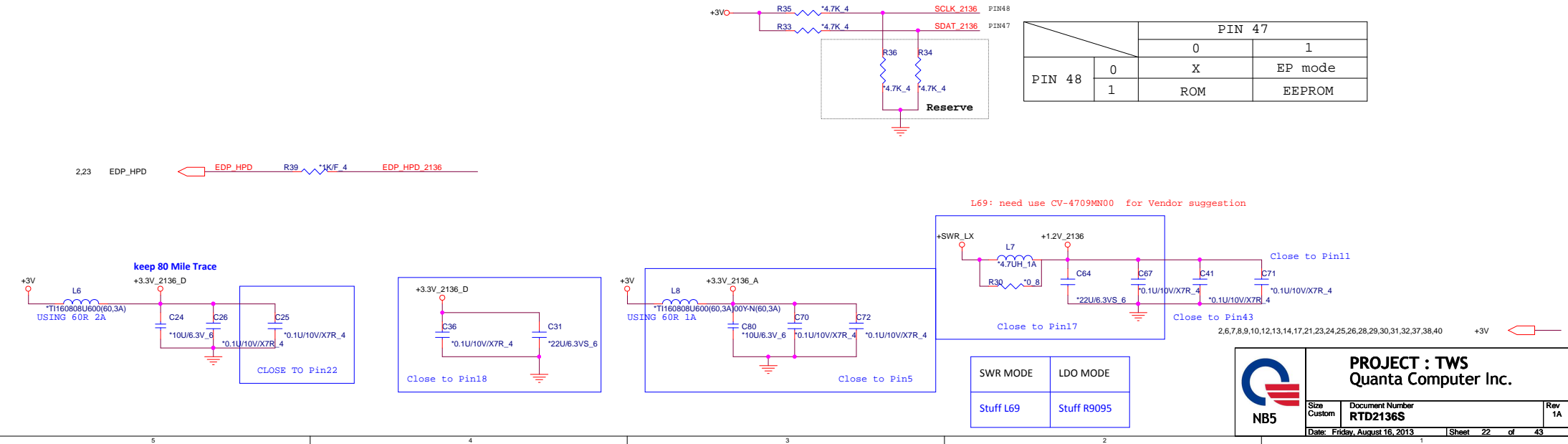
## EMI request





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		PIN 47	
PIN 48	0	X	EP mode
	1	ROM	EEPROM

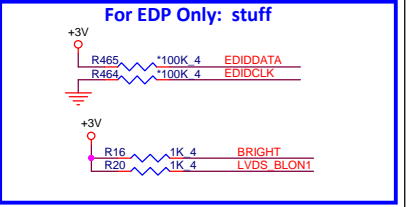
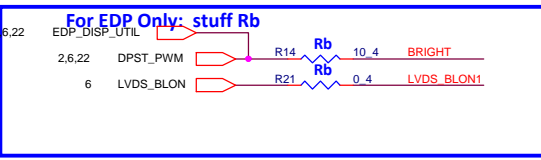
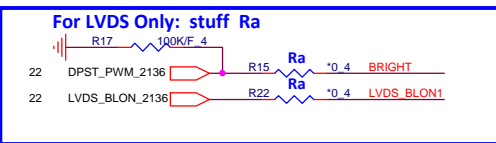
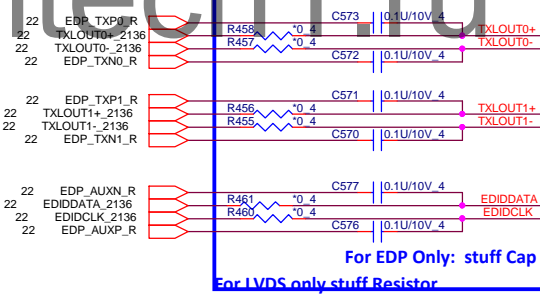
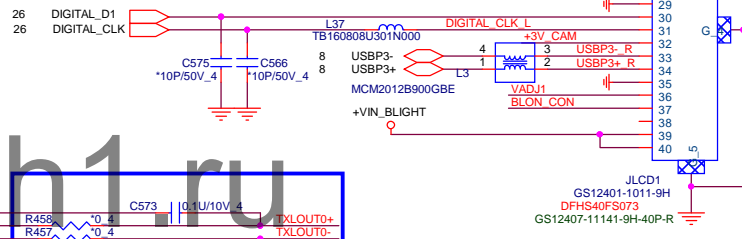
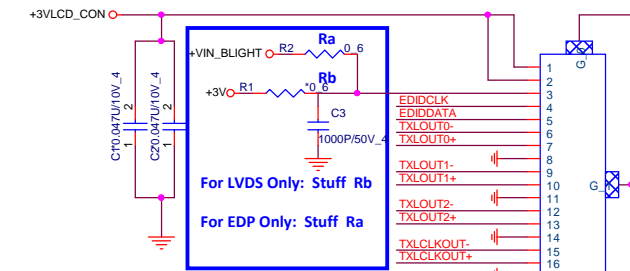
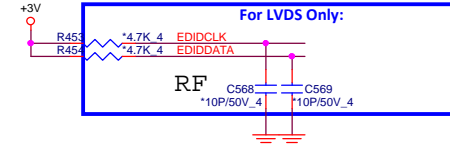
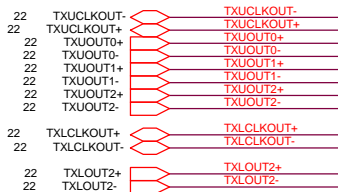
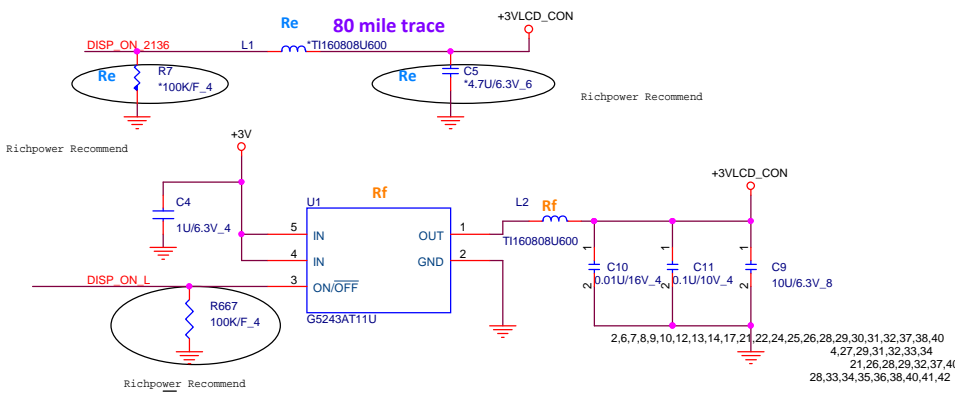
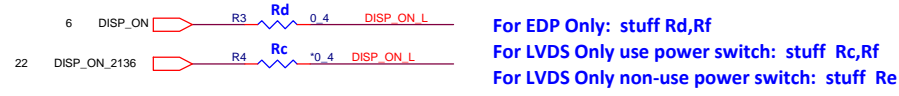
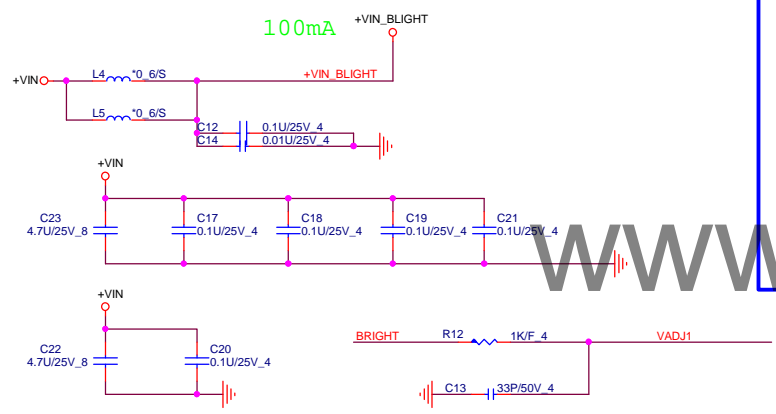
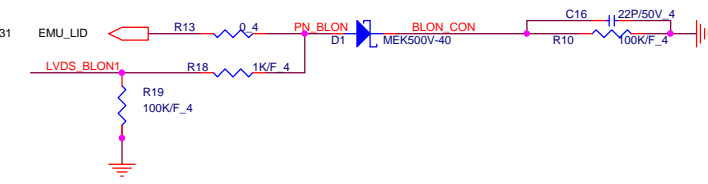


**PROJECT : TWS**  
Quanta Computer Inc.

Size Custom	Document Number <b>RTD2136S</b>	Rev 1A
Date: Friday, August 16, 2013	Sheet 22 of 43	

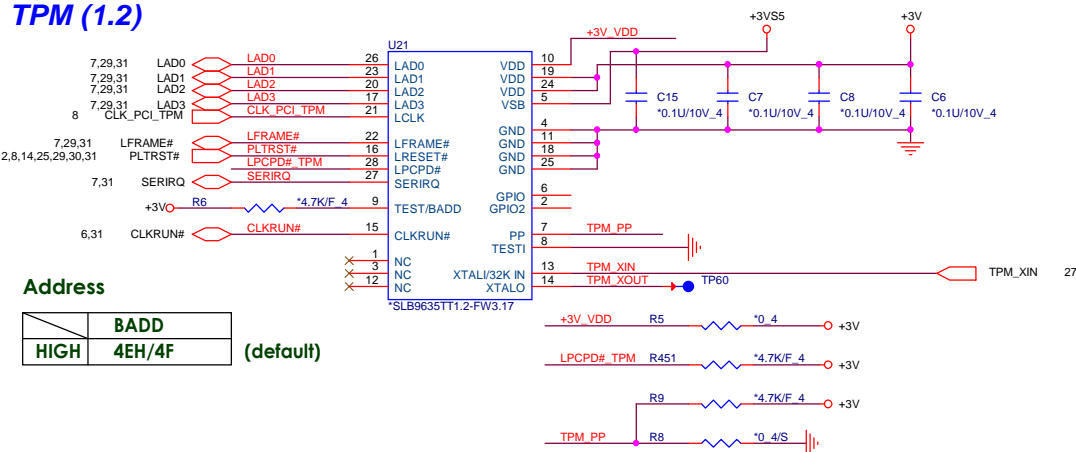
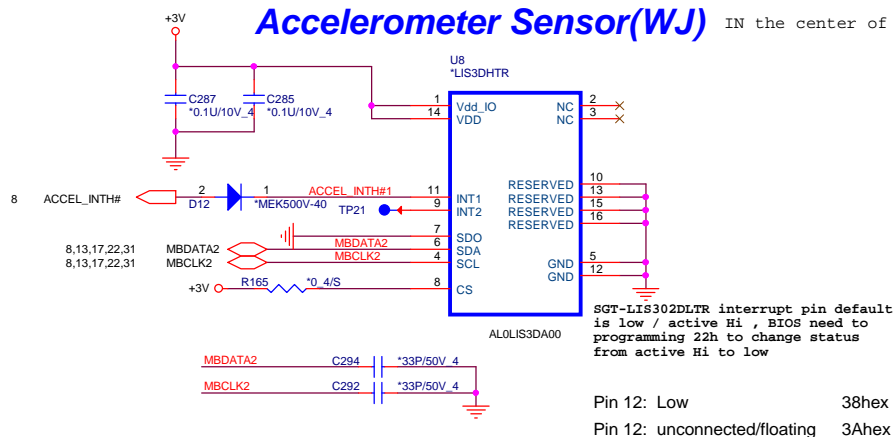
# LID Switch

23



PROJECT : TWS  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A
Date: Friday, August 16, 2013	Sheet 23 of 43	

**TPM (1.2)****Finger Printer****Accelerometer Sensor(WJ)** IN the center of main board

2,6,7,8,9,10,12,13,14,17,21,22,23,25,26,28,29,30,31,32,37,38,40  
4,27,29,31,32,33,34  
21,26,28,29,32,37,40

+3V  
+3VPCU  
+5V

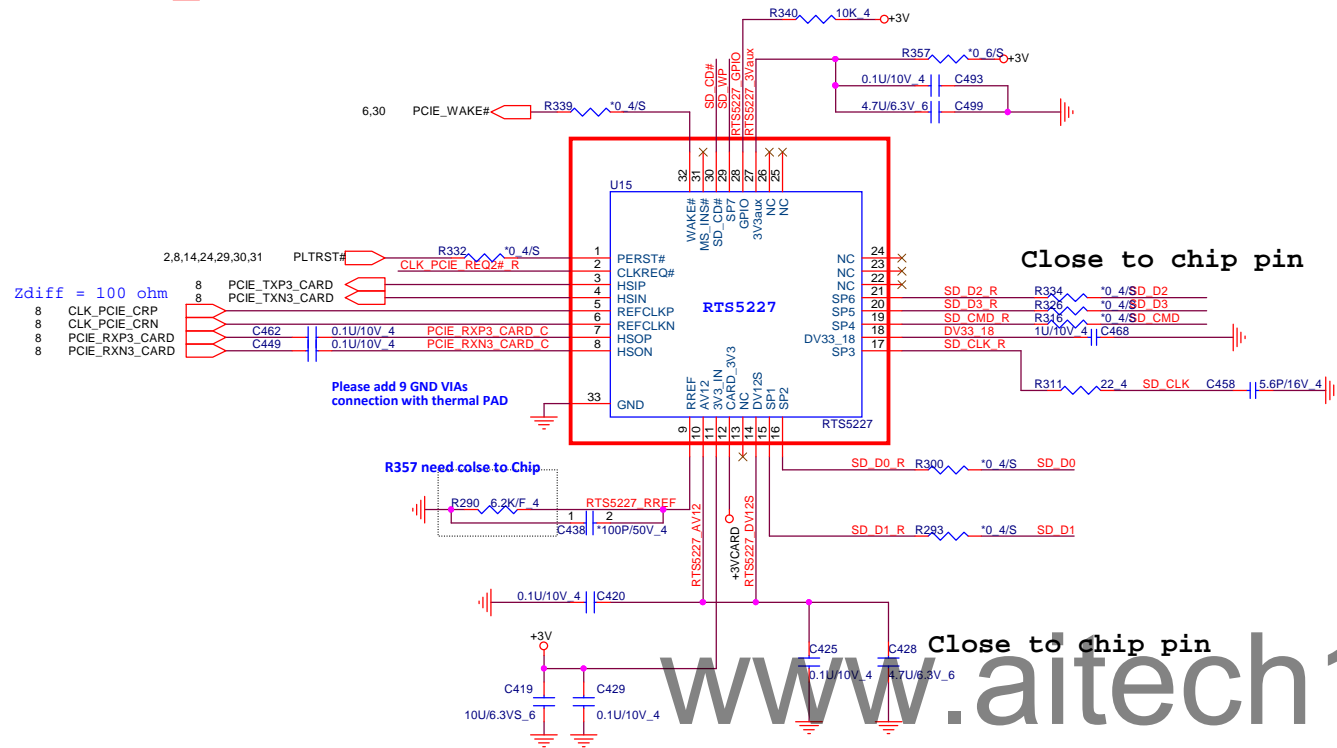


**PROJECT : TWS**  
**Quanta Computer Inc.**

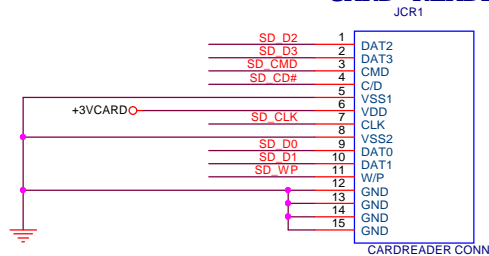
Size Custom	Document Number <b>TPM/FP/G Sensor</b>	Rev 1A
Date: Friday, August 16, 2013	Sheet 24 of 43	



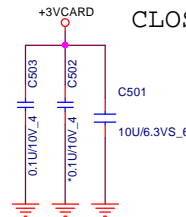
8 PCIE\_CLKREQ\_CR# \*0 4/S CLK\_PCIE\_REQ2# R



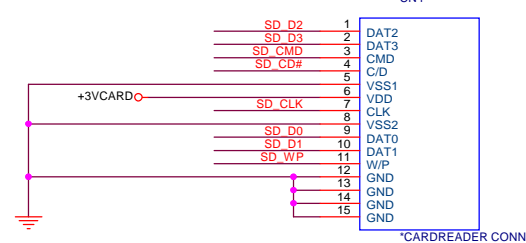
### 15" ONLY SD / MMC CARD READER



### CLOSE CONN



### 14" ONLY SD / MMC CARD READER



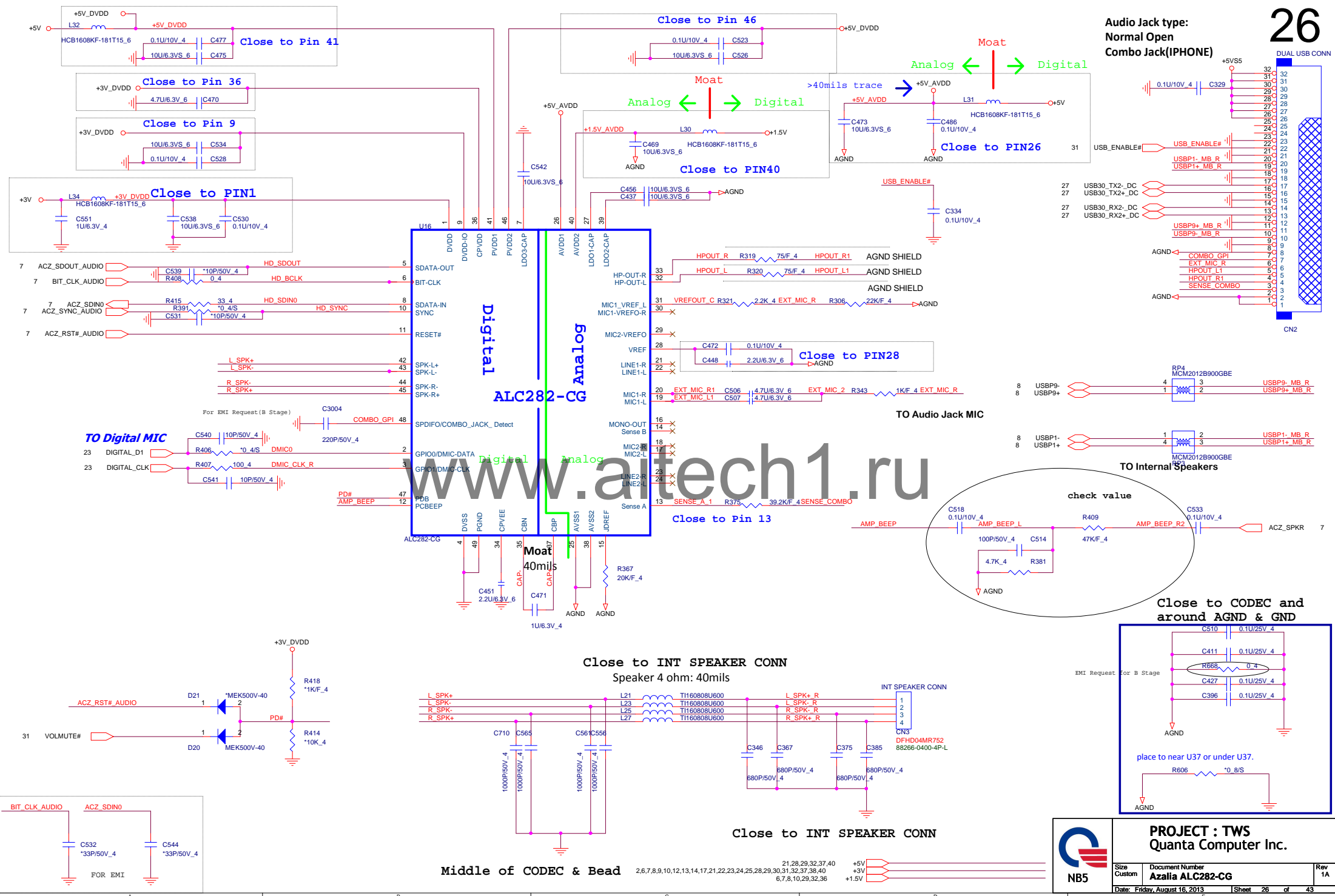
2,6,7,9,10,24,27,28,29,31,34,36,37,42  
2,6,7,8,9,10,12,13,14,17,21,22,23,24,26,28,29,30,31,32,37,38,40

+3VSS  
+3V




PROJECT : TWS  
Quanta Computer Inc.

Size Custom	Document Number RTS5227 & CR SOCKET	Rev 1A
Date: Friday, August 16, 2013	Sheet 25 of 43	



Audio Jack type:  
Normal Open  
Combo Jack(IPHONE)

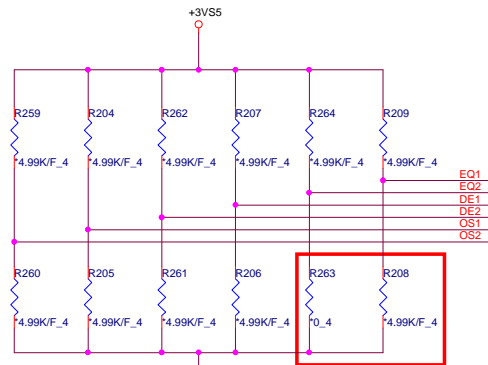
26



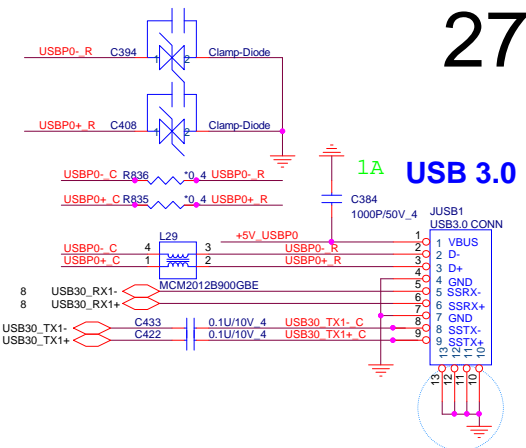
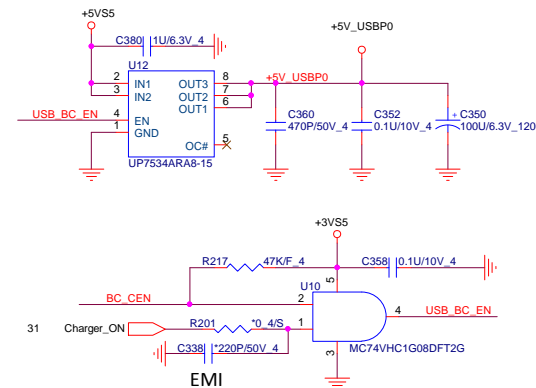
**PROJECT : TWS**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	Azalia ALC282-CG	1A
Date: Friday, August 16, 2013		Sheet 26 of 43

## USB3.0/USB2.0 COMBO



OSx		Transition Bit Amplitude	
NC(default)		1000	
0		870	
1		1085	
EQx		Equalization dB	
NC(default)		0	
0		7	
1		15	
DEX	OSx=NC	OSx=0	OSx=1
NC	-3.5dB	-2.2dB	-4.4dB
0	-6.0dB	-5.2dB	-6.0dB
1	-8.5dB	-8.9dB	-7.6dB
EN_RXD		DEVICE FUNCTION	
1(default)		Normal operating mode	
0		Sleep mode	
CM		DEVICE FUNCTION	
0(default)		Normal operating mode	
1		Compliance mode	



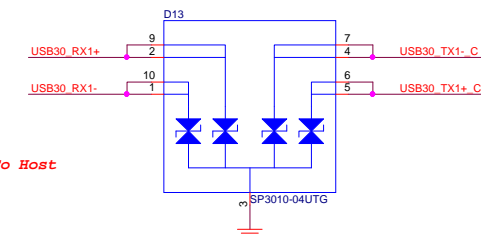
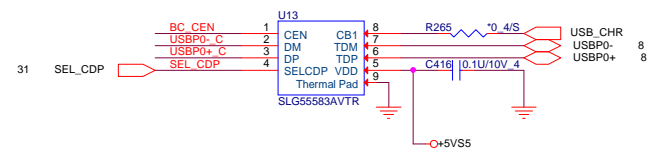
PV : change for NXP re-driver IC setting  
add R696/R695 for TI signal measure

HOST

## USB3.0 re-driver IC

**DEVICE**

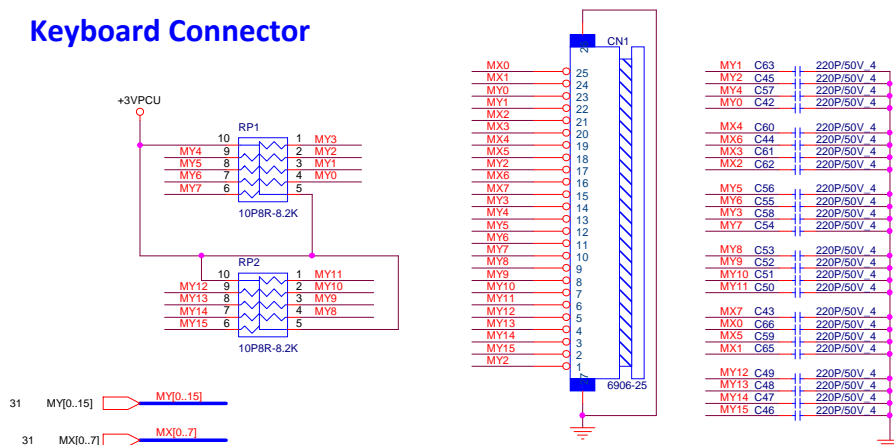
## Charge USB



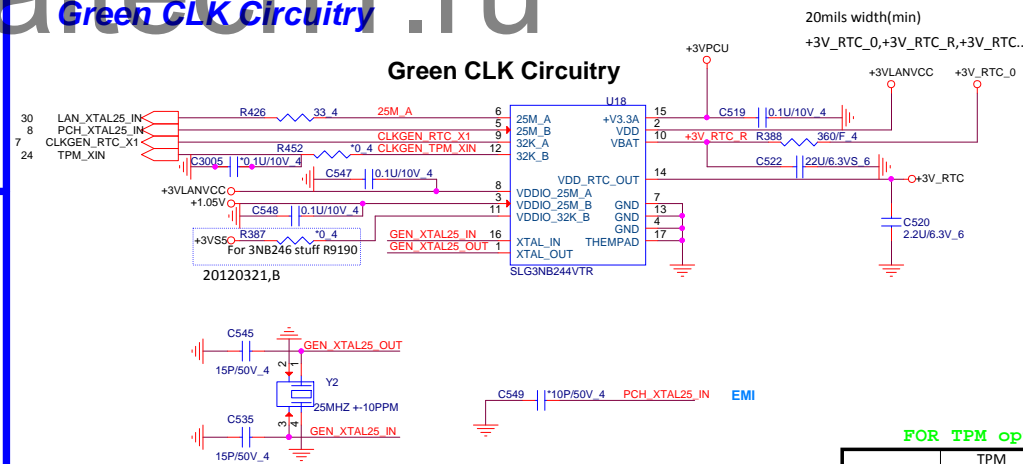
Green CLK Circuitry

## Green CLK Circuitry

## Keyboard Connector



### Green CLK Circuitry



FOR TPM option

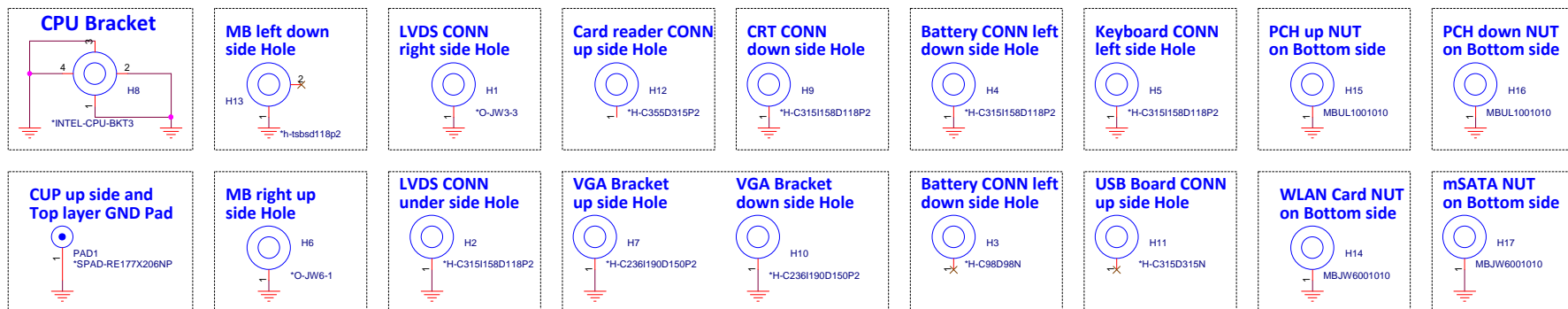
	TPM	Non-TPM
<b>R525</b>	Stuff	NA
<b>U5</b>	AL3NB246000	AL3NB244000



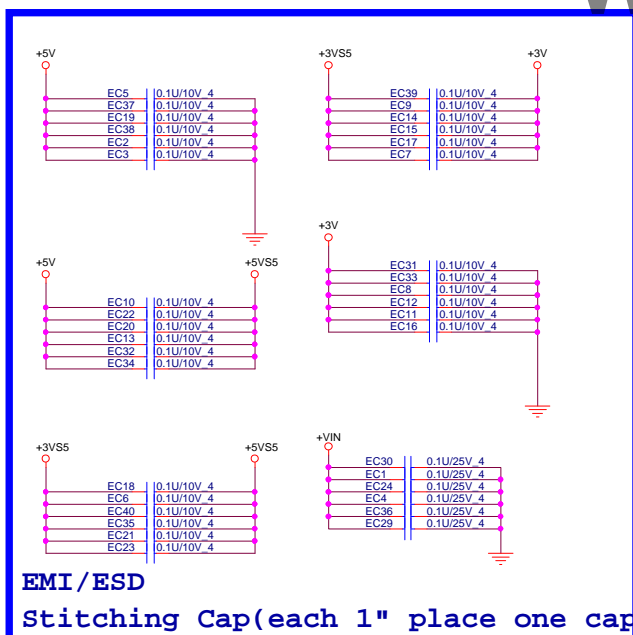
**PROJECT : TWS**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>USB3.0/Charge USB/KBD/Green CLK</b>	Rev 1A
Date: Friday, August 16, 2013		Sheet 27 of 43

## Hole

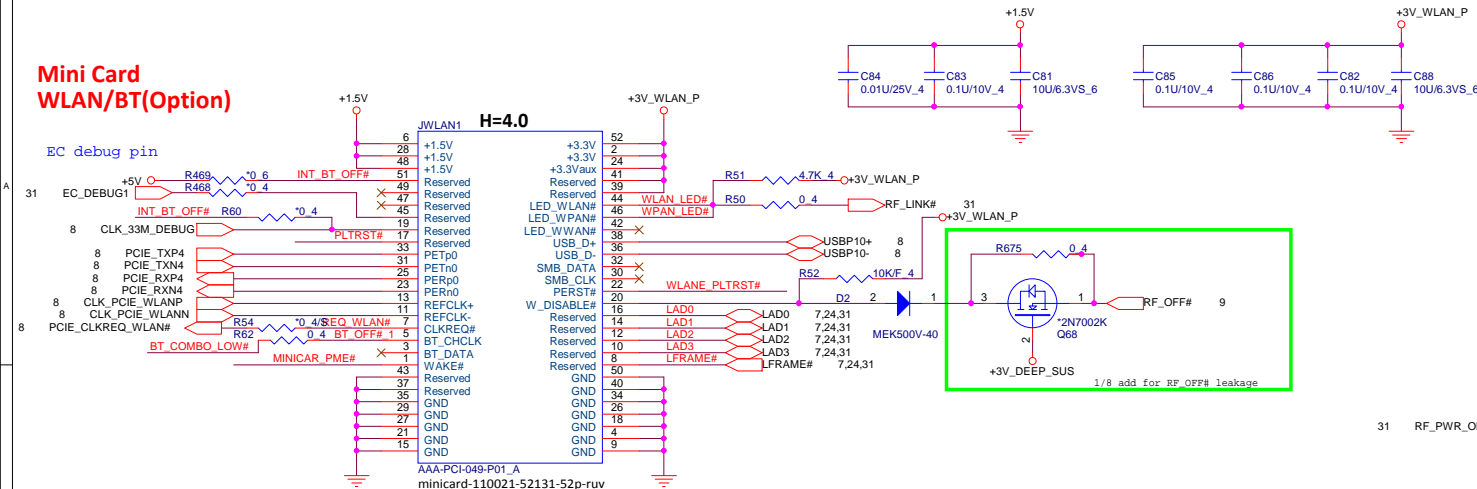


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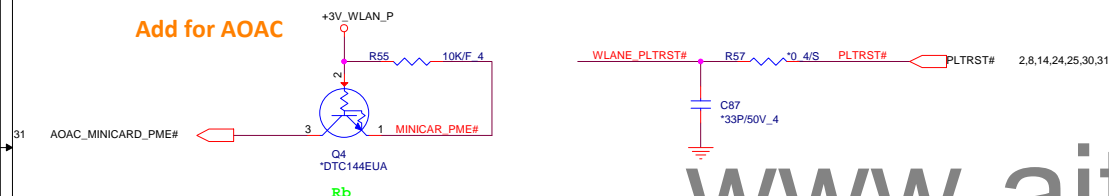
## Mini Card WLAN/BT(Optional)

EC debug pin



## Support Wake Function(Reserve)

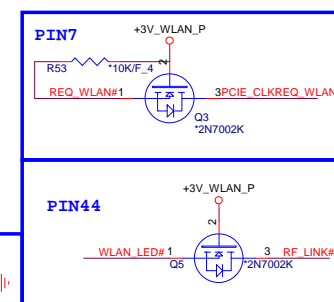
Add for AOAC



## Mini Card Reset

non-AOAC	LG	Ra
AOAC	CB	Rb

Avoid leakage issue

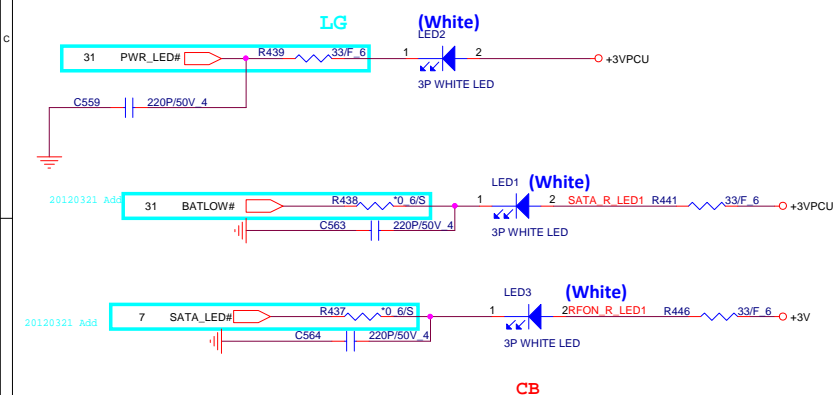


For EMI Suggestion

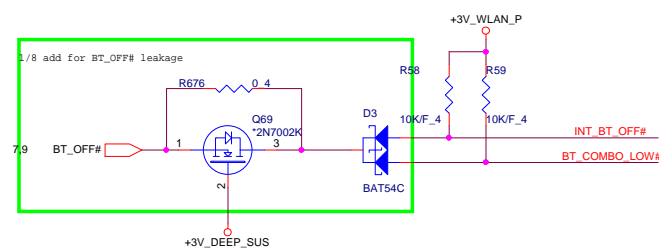
CLK\_33M\_DEBUG R61 0.4 C89 33P/50V\_4

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## LED Status



PIN19, 51



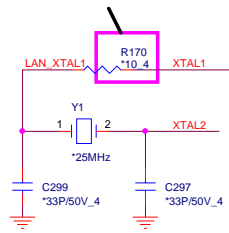
9/4 Intel COMBO card control circuit  
1.add R1001,R1002,Q1001  
2.add net name "INT\_BT\_COMBO\_EN#" -> "INT\_BT\_OFF#"

2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,26,28,30,31,32,37,38,40  
21,26,28,32,37,40  
4,27,31,32,33,34  
6,7,8,10,26,32,36

+3V  
+5V  
+3VPCU  
+1.5V



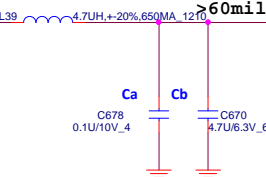
For EMI 0 ~ 22 ohm



Power trace Layout 宽度 &gt; 60mil

next ver need to add 0805 0 ohm &amp; 0.1u cap for 10/100

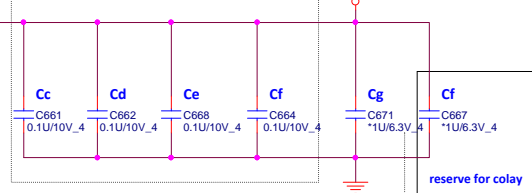
&gt;60mil

Trace < 30 mil  
Width > 60 milFor GbE  
Stuff La, Ca, CbFor 10/100  
NA: La, Ca, Cb

For GbE

\* Place Cc, Cd, Ce, Cf  
close to each VDD10 pin-- 3, 8, 22, 30

For 10/100 NA Ce, Cf

\* Place Cc, Cd  
close to each VDD10 pin-- 8, 30 only,

For GbE

\* Place Cg close to each VDD10 pin-- 22 (reserve)

For 10/100

\* Place Cf close to each VDD10 pin-- 30 (reserve)

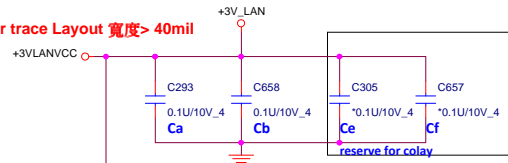
For 10/100

\* Stuff Ce and Cf only, close to each VDD33 pin-- 23, 32

For GIGA

\* Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32

Power trace Layout 宽度 &gt; 40mil



\* Place Cc and Cd close to each VDD33 pin-- 23, 32

For GIGA

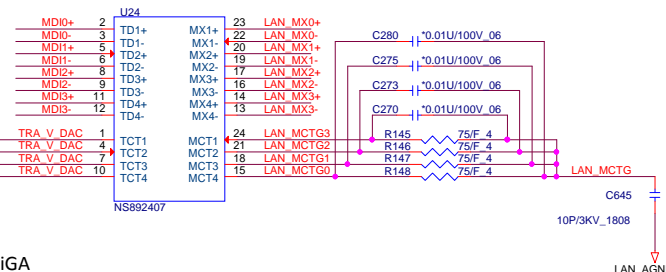
Stuff Cc, Cd

For 10/100

NA: Cc, Cd

Remove For Not Using SWR mode

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For GiGA

BOT: GST5009B LF, DB0Z06LAN00

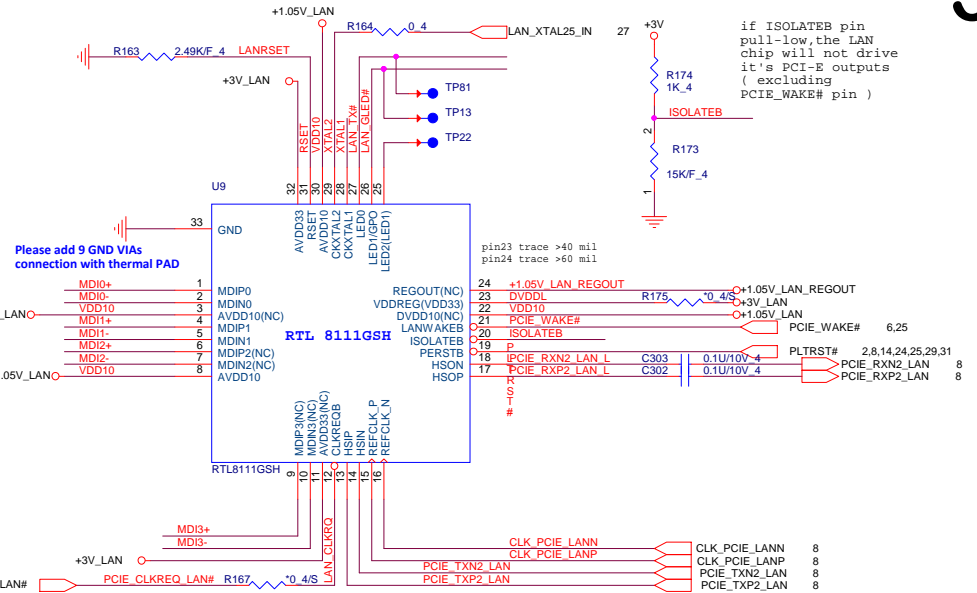
For 10/100

BOT: TST1284R LF DB0EL5LAN00

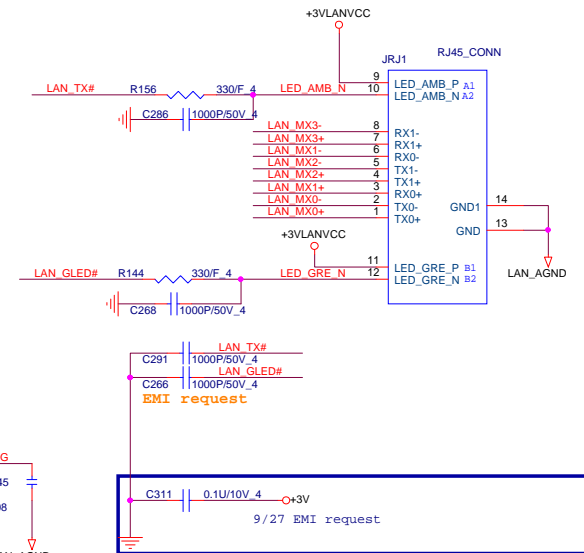
2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,26,28,29,31,32,37,38,40  
27,37

+3V

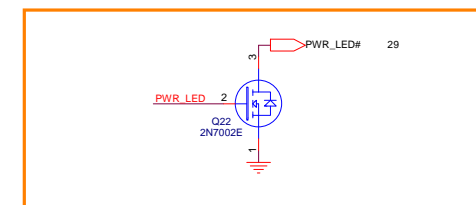
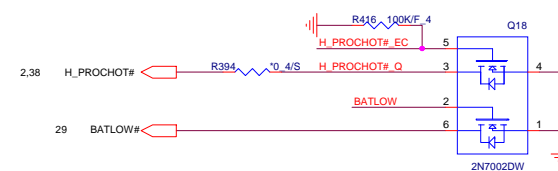
+3V\_LANVCC



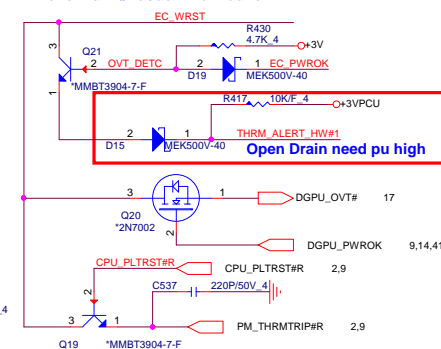
LAN conn

PROJECT : TWS  
Quanta Computer Inc.

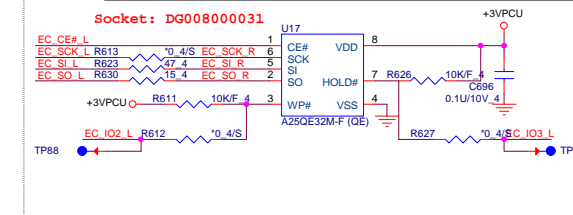
Size	Document Number	Rev
Custom	RTL 8111GS/RJ45	1A
Date: Friday, August 16, 2013	Sheet 30 of 43	



thermal shutdown circuit



Vender	Size	P/N
WIN	4MB	AKE39FN0N01 (WIN W25Q32FVSSIQ (QE)
AMIC	4MB	AKE39ZN0800 (AMIC A25QE32M-F (QE)
Socket		DFHS08FS023



**PROJECT : TWS**  
**Quanta Computer Inc.**

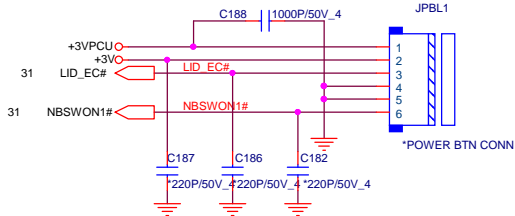
Size Custom	Document Number <b>EC (ITE8258E)/ROM</b>	Re
Date: Friday, August 16, 2013	Sheet 31 of 44	

2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,26,28,29,30,32,37,38,40  
2,4,9,10,27,35,42  
+1.05V  
+3V  
+3VPCU

## Left side Power Button Connector

Pin1 : +3VPCU(LIDSWITCH PWR)  
Pin2 : POWER LED  
Pin3 : LIDSWITCH  
Pin4 : GND  
Pin5 : GND  
Pin6 : POWERON#

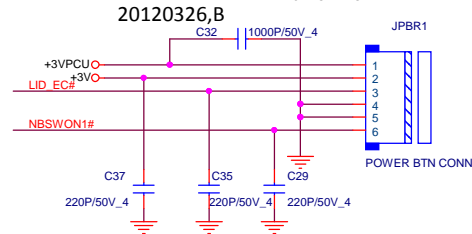
For LG



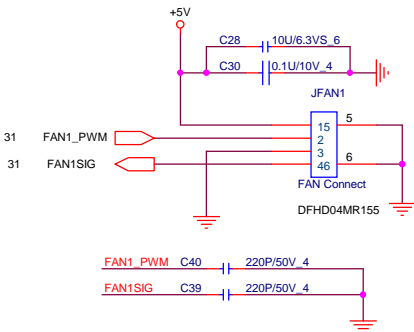
## Right side Power Button Connector(2)

Pin1 : +3VPCU(LIDSWITCH PWR)  
Pin2 : POWER LED  
Pin3 : LIDSWITCH  
Pin4 : GND  
Pin5 : GND  
Pin6 : POWERON#

For CB

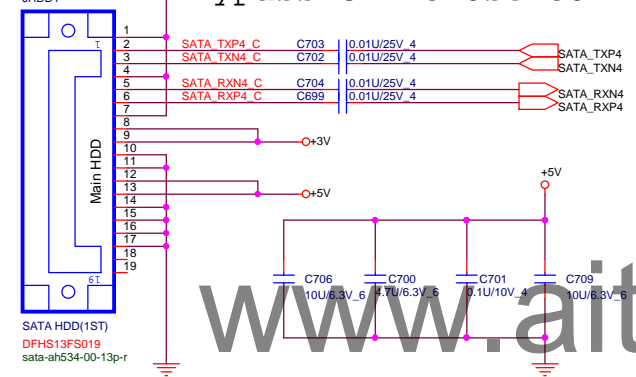


## CPU FAN



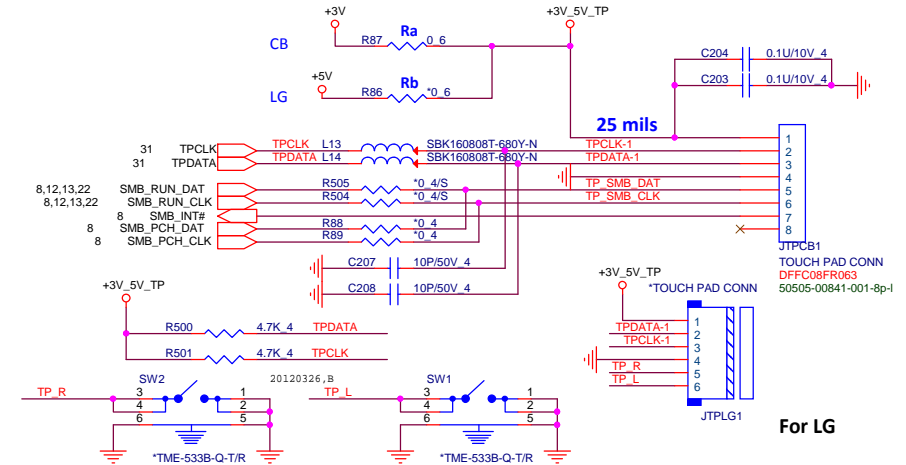
## SATA HDD CONNECTOR

Bypass CAP close conn



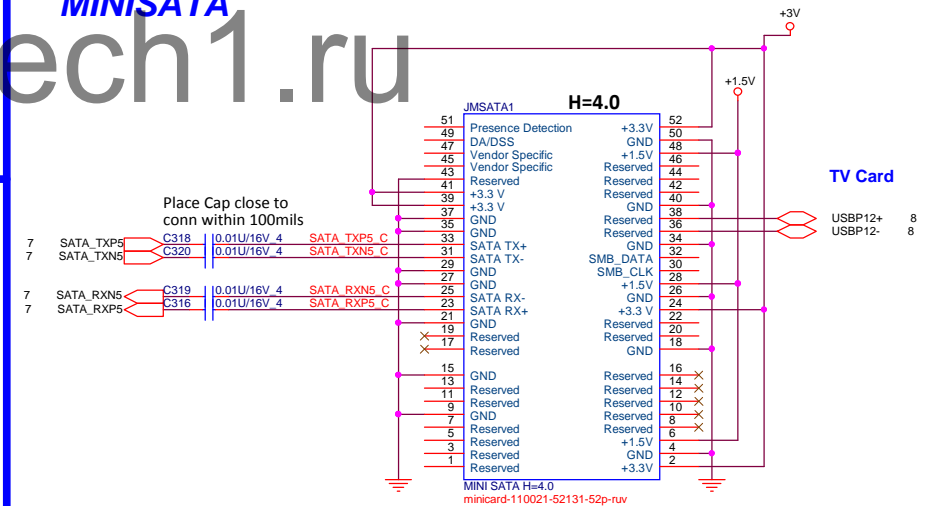
## Touch Pad Connector

	Ra	Rb	JTPCB1	JTPLG1, SW1, SW2
CB	V	X	V	X
LG	X	V	X	V



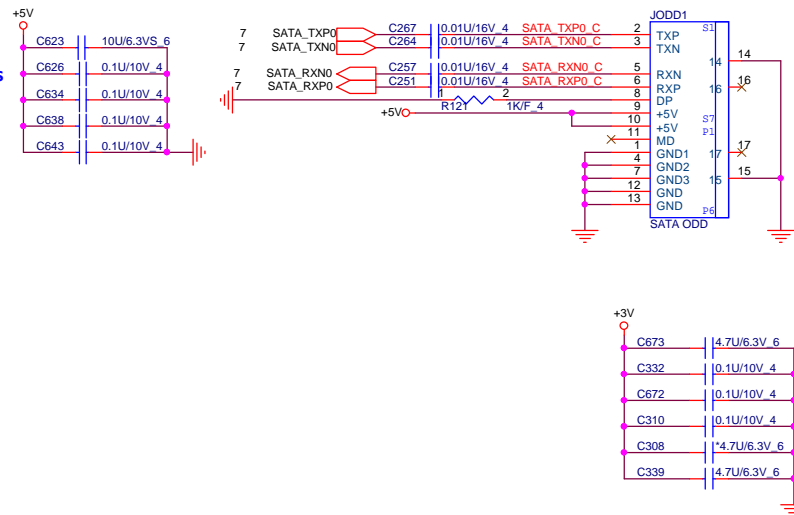
## MINISATA

Place Cap close to conn within 100mils



## SATA ODD Connector

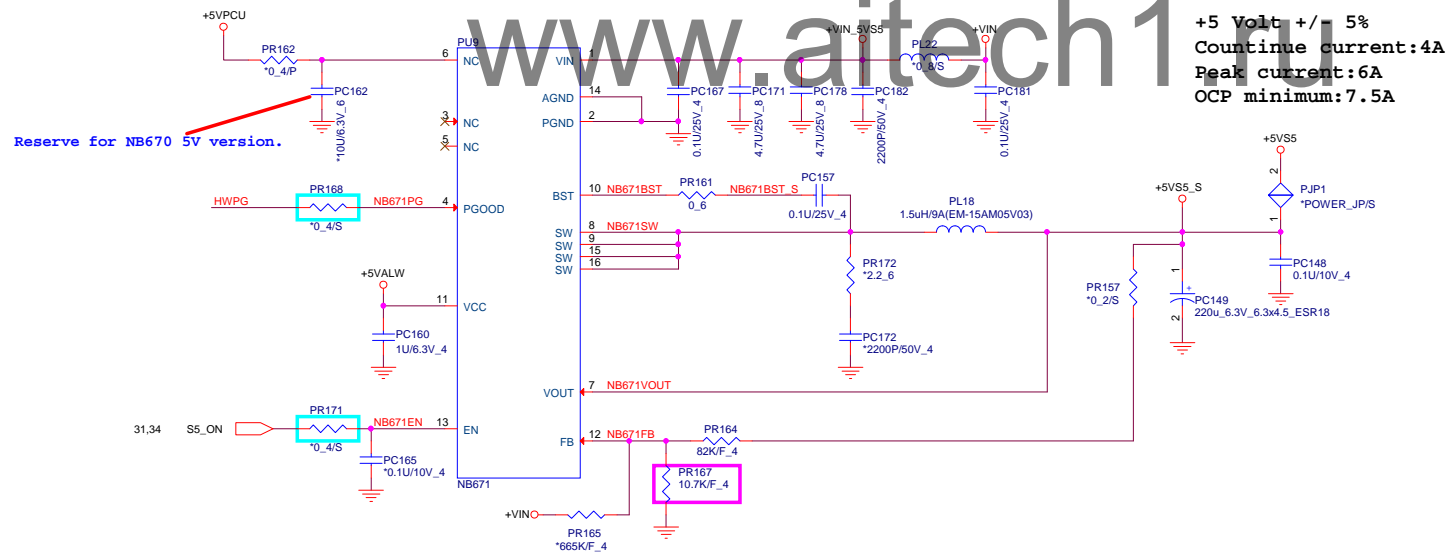
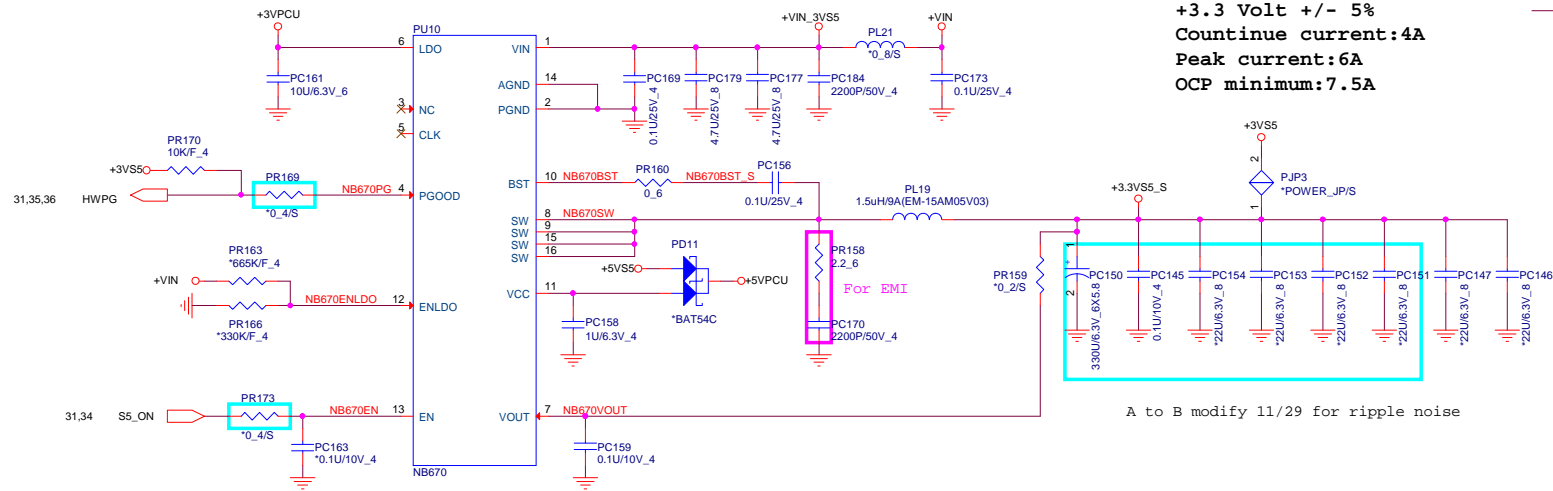
120 mils



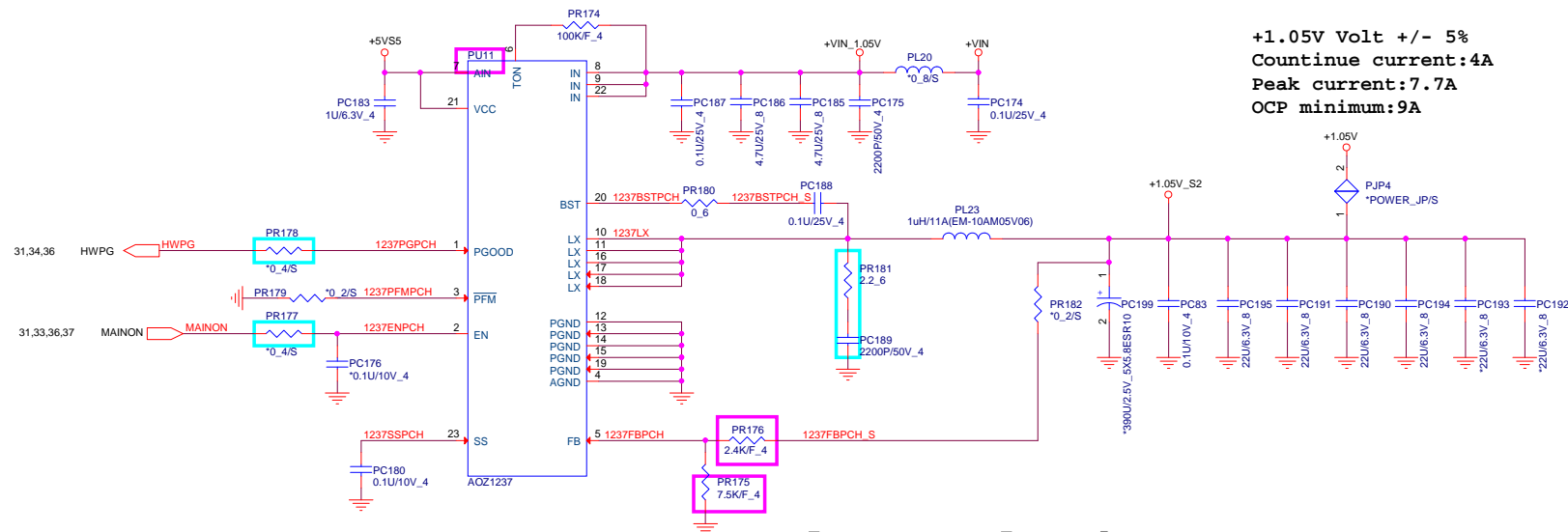
## TV Card

USBP12+ 8  
USBP12- 8



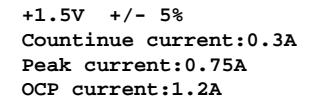


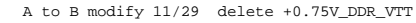





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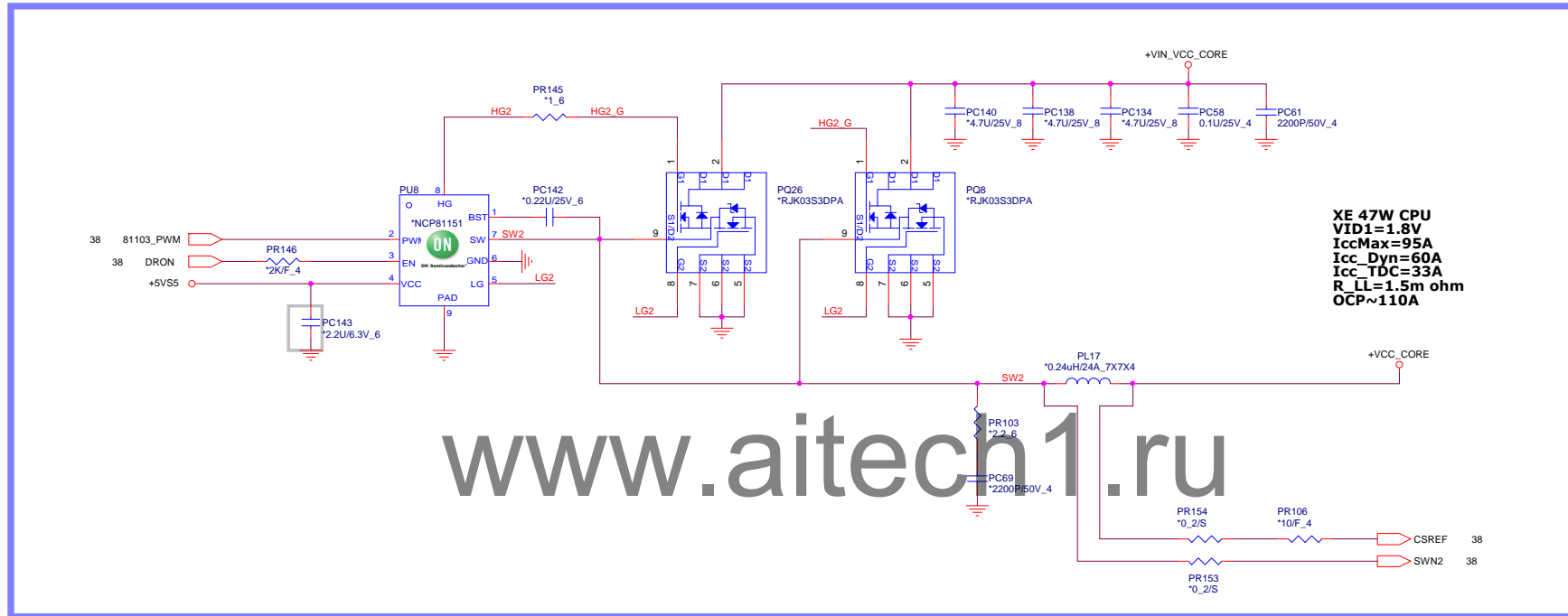
+1.05V 2,4,9,10,27,42






 NB5	<b>PROJECT : TWS</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number Dis-charge IC (G5934)	Rev 1A
	Date: Friday, August 16, 2013	Sheet 37 of 43	





+VCC\_CORE 4,38

		<b>PROJECT : TWS</b>	
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